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LE DIPLOME DE MASTER

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Par

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Intitulé

Analyse et commande des onduleurs multiniveaux monophasés de type PUC

Evalué le : ……

Par la commission d'évaluation composée de :

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- Procès-verbal de la réunion de l'équipe du domaine des Sciences et Technologies du mois de Mai 2021.

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University of Mohamed El-Bachir El-Ibrahimi - Bordj Bou Arreridj

Faculty of Science and Technology

Department of Electronics

Presented to obtain

THE DIPLOMA OF MASTER

FIELD: **Electronics**

Speciality: Electronic Industries

by

- **MERMOUNE Faycel**
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Entitled

Analysis and control of single-phase multilevel PUC inverters

Evaluated on : ……

By the evaluation committee composed of :

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Dedication

To our fathers……. For their unlimited support

To our Teachers ……..... For help me until the end

To our friends ……. Who give us Positive Sentiment.

Acknowledgement

First and foremost, all praise and thanks be to almighty ALLAH for giving me health, wisdom, and patient, without him nothing of my work would have been done.

We would like to express our sincere gratitude to our supervisor Dr. TALBI Billel for his, suggestions and valuable directions. We would like to express our thanks to our co-supervisor, Dr. SAHLI Abdeslem, for his comments and suggestions during the writing of this thesis.

We are aware that we have been honoured by the president of the jury and the examiner for agreeing to review this work.

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List of Acronyms and symbols

AC Alternative current

HB Half-bridge

FB Full-bridge

THD Total of harmonic distortion

MLI Multi-level inverter

CHB Cascade h-bridge

NPC Neutral point clamped

FC Flying capacitor

PUC Packed unit cell

MPC Model predictive control

PI Proportional integral

GW Gigawatt

PWM Pulse width modulation

PLL Phase-locked loop

Lf Filter inductance

Vdc DC-link voltage

Cdc DC-link capacitor

Ig* grid reference current

ig grid current

vs Grid voltage

g Cost function

R load resistor

F Grid frequency

L Rectifier side load inductor

Iload Load current

Sa, b,c, Switching signals of the inverter Vs Grid voltage

Ts MPC sampling time

PI Proportional integral

General Introduction

Nowadays, multilevel inverters (MLIs) are in rapid development and have become a very useful solution [1]. A lot of publications have been introduced the most common MLI topologies like Cascaded H-Bridge (CHB), Flying Capacitor(FC), Neutral-Point Clamped(NPC), and Packed U-Cells (PUC) inverters. PUC inverter (classified as FC inverter) has a lot of advantages compared with other MLI topologies such as high power quality, the ability and flexibility in the multilayer voltage synthesis, simple construction, reduced number of switches and DC sources reliability and less cost. Because the PUC topology uses only one DC source, the capacitor voltage must keep balance at the reference value. Many control techniques for PUC inverters have been suggested, like hysteresis controller, proportional-integral (PI), and Model Predictive Control (MPC), it was not used widely due to high computational cost, but recently, the rapid development in digital signal processors has become the common solution [2].

This thesis aims to study PUC multilevel converter topologies with effective control method in order to reduce the total harmonic distortion (THD) in the output waveform by increasing the number of voltage levels, reduce the voltage stress on the switches, decrease the size of the inverter by reducing the filter size, achieve the stability under step change in the injected current to the grid and parameters mismatching.

In this regard, five and nine level PUCs with finite-control-set model predictive control (MPC) have been modeled and simulated in this work. Different testing and parameters change cases have been tested to verify the validity of used approach and to make sure that the objectives have been achieved. A brief outline of the thesis is given below:

- The first chapter introduces the most popular of signal phase multilevel inverter topologies and control approaches, as well as some comparisons between them.
- The second chapter shows the PUC5 and PUC9 topologies, and MPC control technique, including model prediction, state variable normalization, and cost function calculation. It demonstrates the robustness analysis of the suggested model as well as the simulation results of model predictive control compared with conventional control technique (based on PI with PWM) using Matlab/Simulink software.

Finally, a general conclusion of this thesis and perspectives conclude this work.

Chapter I:

Overview Of Single-Phase Multilevel Inverters Topologies

I.1. Introduction

Multilevel converters have emerged as the most significant advancement over conventional converters; which could only produce a two-level voltage waveform at the output. The two-level waveform has a lot of harmonics, which needs the use of bulky filters to eventually generate a sinusoidal voltage waveform.

Multilevel converter can produce different voltage levels using combinations of switches and DC sources. The numerous levels reform the voltage waveform into a quasi-sine wave with low harmonic components. Therefore, the need of large filters to eliminate voltage harmonics is removed. On the other hand, dividing the voltage between switches makes it easier to use multilevel converters in high-power applications using only medium voltage switches [1].

In this chapter, some of the most common single-phase multilevel inverters will be presented, followed by a quick comparison between them to explain our decision to use the packed U cell (PUC) inverter topology for our work.

I.2. Multilevel inverter

Several semiconductor switches and DC supply are included in a multilevel inverter. The output voltage levels are produced by a combination of switch operations. The basic principle of a multilevel inverter functioning is depicted in Figure I.1. In two-level, three-level, and *n*-level configurations, it indicates the DC link and one leg of the inverter [1].

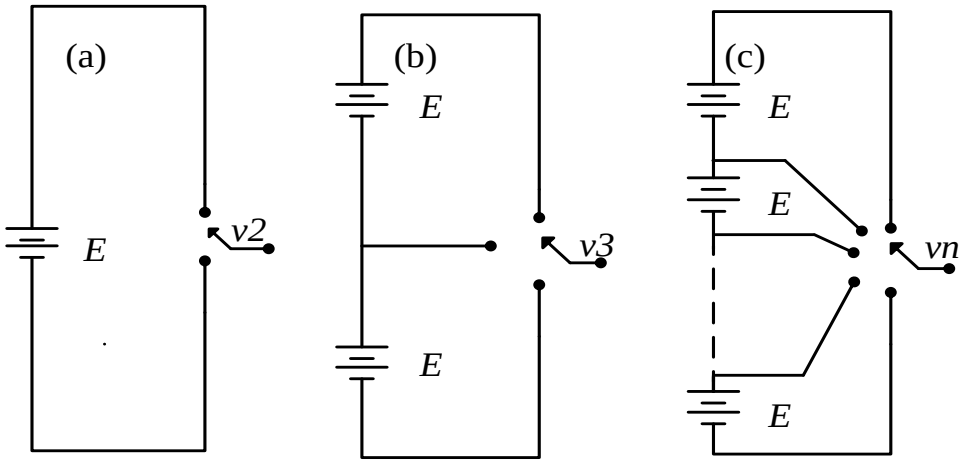


Figure I.1: One leg of, (a) 2-level, (b) 3-level and (c) n-levels inverter

Figure I.1(a) depicts a conventional inverter that can produce +*E* or –*E* at the output point with respect to the grounded neutral point, while Figure I.1(b) depicts a three-level inverter that produces +*E*, 0 and – *E* at the output, and Figure I.1(c) depicts a n-level inverter that generates multilevel voltages of 0,± *E*, and ±*2E*….

The semiconductor switches, as shown in Figure I.1, are only exposed to *E* or less, but the output may be higher than *E*. This characteristic of a multilevel inverter aids industry and renewable energy resources in supporting high power needs and applications by utilizing medium-voltage equipment.

Due to its appealing qualities, multilevel inverters have lately attracted the attention of researchers and industry. The following are some of the most significant advantages of multilevel inverters:

- Reduced output voltage distortion due to various output waveform levels.
- Used for High power applications.
- Lower switching frequency results in lower switching losses.
- Low harmonic voltage/current waveforms.

I.3. Single-phase multilevel inverter topologies

For single-phase multilevel inverters, various topologies have been proposed, which are presented following.

I.3.1. Cascaded H-bridge

This topology can be used for medium and high power applications; the cascade H-Bridge (CHB) multilevel inverter is most commonly utilized. The CHB is made up of numerous units of single-phase H-Bridge inverters connected in series [1]. The output voltage levels, depending on the number of DC sources, will be able to range from *-mE* to *mE*, with *2m + 1* levels. Where m is the number of distinct DC sources. Increasing the number of levels results in a virtually sinusoidal output voltage waveform. Even without applying any filters, increasing the number of levels causes the output voltage waveform to become almost sinusoidal. Figure I.2 illustrates a single-phase five-level CHB, which contains two single-phase HB cells. In this case, the five output voltage levels are 0, ±E, and ±2E, which are shown in Figure I.3.

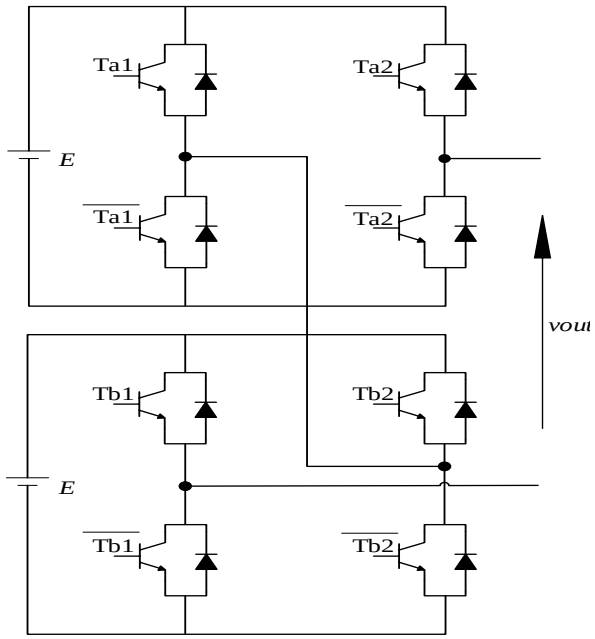


Figure I.2: Single-phase five-level CHB inverter

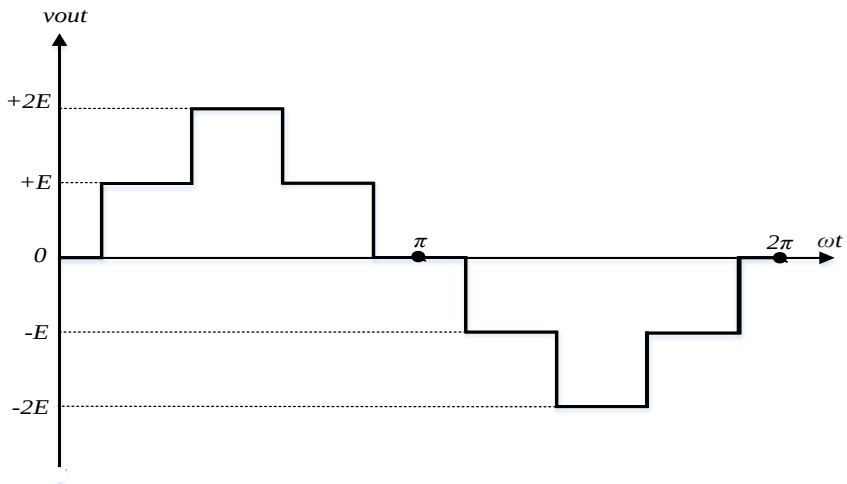


Figure I.3: The output voltage waveform of single-phase five-level CHB inverter

The output voltage levels of the single-phase inverter CHB are listed in Table I.1. The main disadvantage of this topology is the high cost of the inverter, because increasing the number of voltage levels necessitates a large increase in the number of switches and DC sources.

Table I.1: Switching states for five-level CHB Inverter

Switching sequences				Voltage levels
Ta1	Ta2	Tb1	Tb2	*vout*
0	1	0	1	-2E
0	1	0	0	-E
0	0	0	0	0
1	0	0	0	+E
1	0	1	0	+2E

I.3.2. Neutral point clamped

Figure I.4 depicts a five-level single-phase neutral point clamped (NPC) inverter, initially proposed by Nabae, Takahashi et Akagi, 1981. After that, the five-level NPC has found many developments and usage in industries [1].

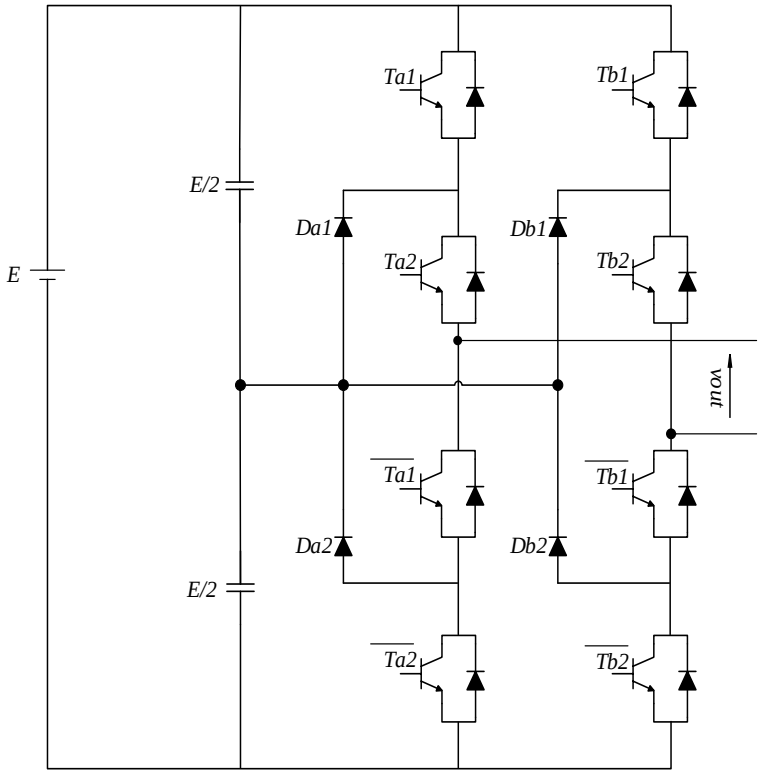


Figure I.4: Single-phase five-level NPC inverter

The clamped diodes (D1a, D2a, D1b, and D2b) are connected to the DC capacitors neutral points, resulting in a zero level addition to the output voltage. In this topology, clamping diodes play a very important role in keeping the switch voltage at the necessary level [1]. The switching state of a five-level NPC inverter is shown in Table I.2.

Table I.2: Switching states for five-level NPC Inverter

Switching sequences				Voltage levels
Ta1	Ta2	Tb1	Tb2	*vout*
1	1	0	0	+E
0	1	0	0	+E/2
0	0	0	0	0
0	0	0	1	-E
0	0	1	1	-E/2

One of the advantages of this structure is its flexibility to be controlled using both PWM and space vector modulation (SVM) [1]. Nevertheless, when the number of voltage levels is very large, the system is hard to construct given a large number of semiconductors necessary (the number of clamping diodes can be written as (*m-1*) (*m-2*), where *m* is the number of levels).

I.3.3. Flying capacitor

The Flying Capacitor (FC) topology is also another multilevel inverter topology proposed by Escalante Vannier and Arzandé, 2002. Figure I.5 presents the topology of three-level FC inverter. This topology has a similar number of switches as the NPC multilevel inverter, but the number of additional capacitors beyond the primary DC-bus capacitors is (*m-1*)(*m-2*)/*2*, where *m* is the number of levels. In addition, it needs a high number of isolators for DC capacitors, as well as a complicated voltage balancing control, limiting its practical application [1]. Table I.3 lists the switching state of a three-level FC inverter.

Table I.3: Switching states for three-level FC Inverter

Switching sequences				Voltage levels
Ta1	Ta2	Tb1	Tb2	*vout*
1	1	0	0	+E
1	0	1	0	0

0	0	0	0	0
0	1	0	1	0
0	0	1	1	-E

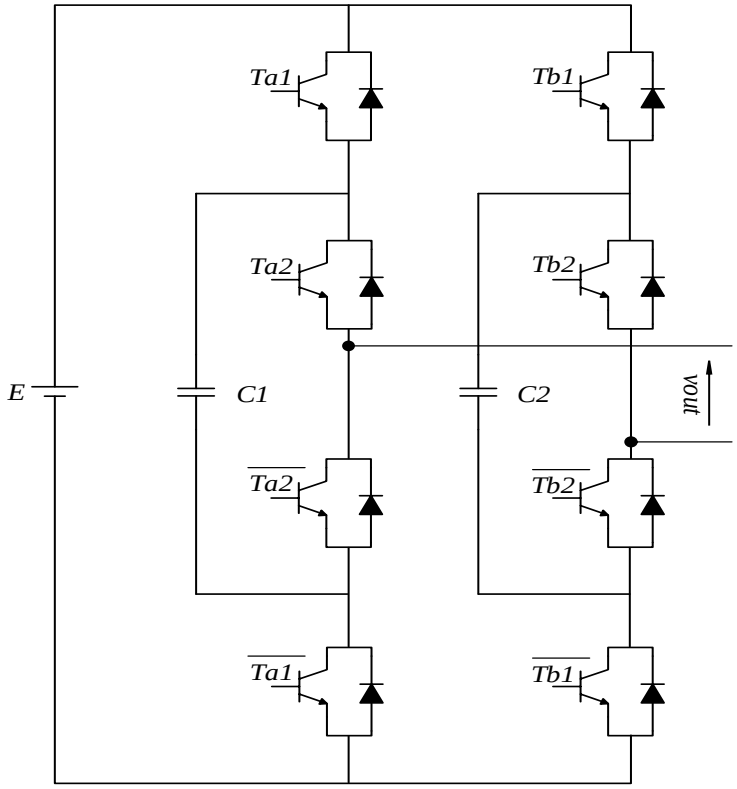


Figure I.5: Single-phase three-level FC inverter

I.3.3. Packed U cell

This topology is a hybridization of FC and CHB with less capacitors and semiconductors. Al-Haddad introduced the PUC converter in 2011, and Vahedi developed it in 2015 [3]. It can be utilized in both single-phase and three-phase configurations.

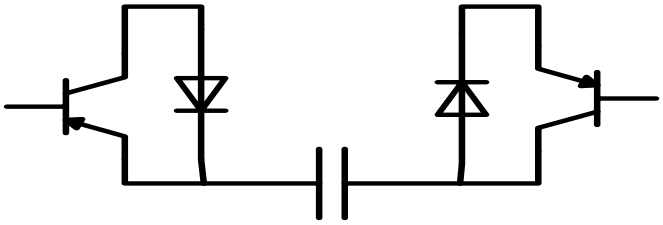


Figure I.6: Single packed U cell

Packed U cells as shown in Figure I.6, each U cell is made up of two power switches and a capacitor. The benefits of the proposed concept will be confirmed in the next chapter by simulation results and experimental validation [3].

I.4. Comparison between different single-phase multilevel inverter topologies

Following the brief descriptions of multilevel inverter topologies, a brief conclusion based on comparative analysis can be given, as shown in Table I.4.

Table I.4: Single-phase multilevel inverter components

***n*: Celle *m*: number of levels**				
Topology	NPC	FC	CHB	PUC
Source DC	(m-1)	1	(m-1)/2	1
No. of clamping diodes	2(m-2)	0	0	0
No. antiparallel diode	2(m-1)	2(m-1)	2(m-1)	$2^{\log_2(m+1)}$
No. of switches	2(m-1)	2(m-1)	2(m-1)	$2^{\log_2(m+1)}$
No. of capacitors	0	(m-2)	0	$\log_2(m+1)-1$
Total Number	7m-9	5(m-1)	(9/2)(m-1)	-

Based on comparison study, a short conclusion can be formulated after the conducted brief descriptions related to multilevel inverter topologies, as shown in Tables I.5 and I.6. In comparison to the other topologies, PUC5 and PUC9 have achieved reliability and lower costs.

Table I.5: Comparison between five-level inverter topologies

Configuration	NPC	FC	CHB	PUC
Source DC	4	1	2	1
No. of clamping diodes	6	0	0	0
No. antiparallel diode	8	8	8	6
No. of switches	8	8	8	6
No. of capacitors	0	7	0	1
Total Number	26	20	18	14

Table I.6: Comparison between nine-level inverter topologies

Configuration	NPC	FC	CHB	PUC
Source DC	8	1	4	1
No. of clamping diodes	14	0	0	0
No. antiparallel diode	16	16	16	8
No. of switches	16	16	16	8
No. of capacitors	0	7	0	2
Total Number	54	40	36	19

I.5 Control of single-phase multilevel inverters

Several control methods have been proposed for the control of signal phase inverters, the most frequently used ones being shown in Figure I.7 [5].

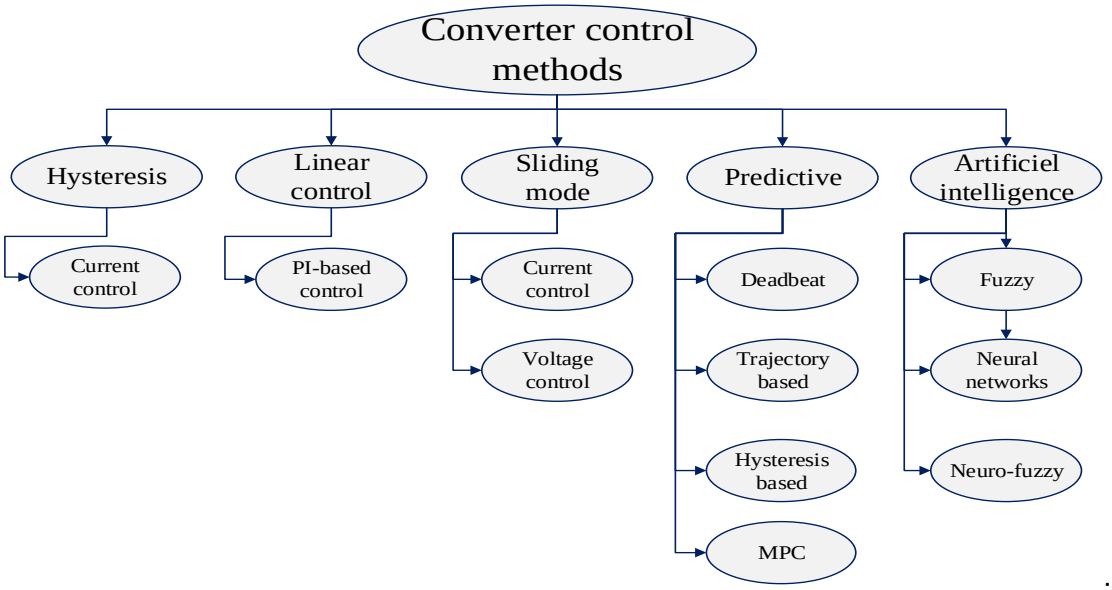


Figure I.7: Different types of a signal phase inverter control schemes

I.5.1. Pulse width modulation (PWM)

The general concept of a pulse width modulator (PWM) is that the reference voltage is compared to a triangular carrier signal and the output of the comparator is used to drive the single-phase multilevel inverter switches. Figure I.8 shown level-shifted PWM, that concept differs from other methods in a small way, for *n*-level multilevel inverter, *n*-1 carrier wave would be compared by sinusoidal wave [1], and the four carrier's waveforms (Cr1, Cr2, Cr3, and Cr4) are shifted vertically to modulate the reference waveform (Vref) completely, which generating a pulsed voltage waveform at the output of the inverter.

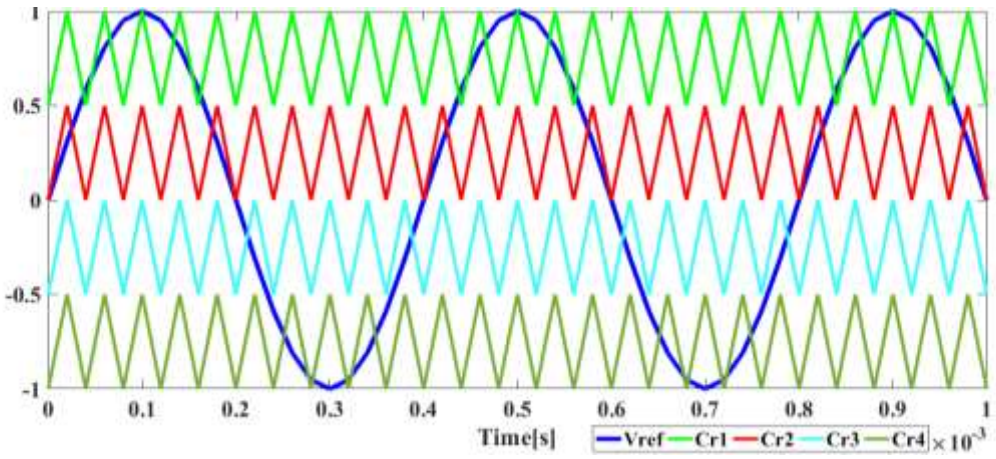


Figure I.8: Level shifted PWM carriers for five-level inverter

I.5.2. Hysteresis current control

The main concept behind hysteresis current control is to keep the current inside the hysteresis band by changing the converter's switching state whenever the current reaches the boundary. Figure I.9 depicts a single-phase inverter's hysteresis control scheme. Here, the current error is used as the input of the comparator and if the current error is higher than the upper limit δ/2, the power switches *T1*, *T4* are turned on and *T2*, *T3* are turned off. The opposite switching states are generated if the error is lower than −δ/2 [5].

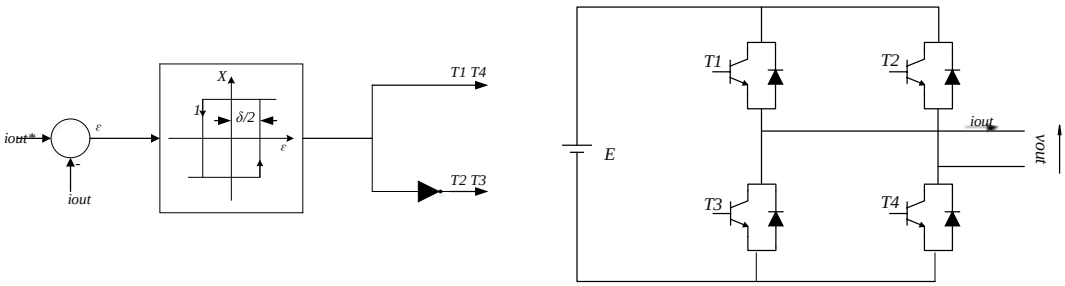


Figure I.9: Hysteresis current control for a single-phase inverter

I.5.3. Model predictive control (MPC)

With the development of faster and more powerful microprocessors, implementation of new and more complex control schemes is possible. Some of these new control schemes for power converters include fuzzy logic, sliding mode control, and predictive control. Predictive control has appeared as an attractive solution for the control of power converters due to its fast dynamic response and increased control accuracy [5].

This is a basic control technique that calculates the control action at each sampling period to provide an optimal value for a related control problem. The applied approach uses a dynamic strategy to forecast future behavior based on the current state of the system. As a result, an

optimal control solution will be found. A basic block diagram of this control technique is given in **Figure I.10**.

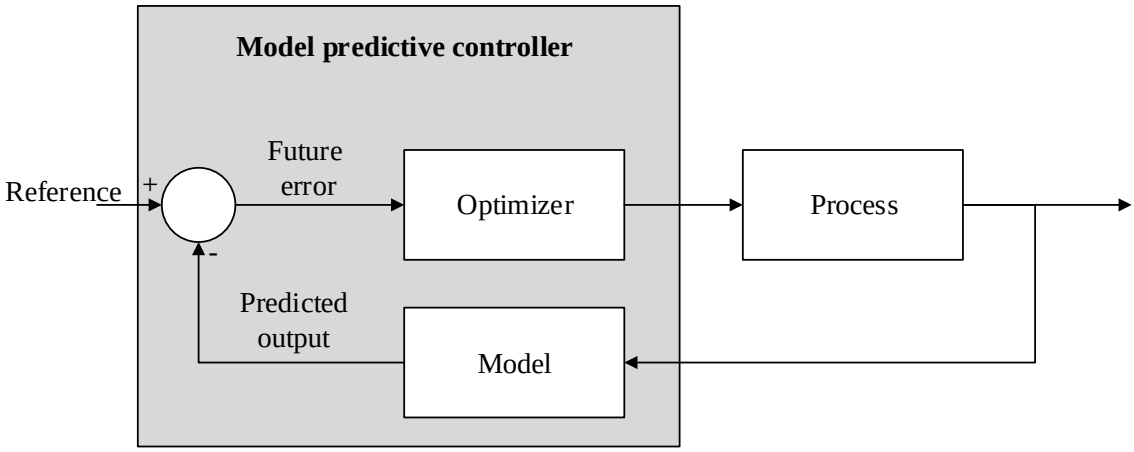


Figure I.10: Block diagram of predictive control

I.6. Conclusion

In this chapter, an overview on single-phase multilevel inverters is presented. The most common topologies are discussed and compared. As results, the PUC topology is quite competitive to other topologies in terms of requiring a small number of capacitors and semiconductor devices, and so avoids bulky installations.

In the following chapter, the PUC5 and PUC9 will be studied and controlled by advanced control technique ‘’ Finite control set model predictive control”.

Chapter II:

Model Predictive Control for 5 and 9-Level Packed U-Cell Inverters

II.1. Introduction

Current control is one of the most studied control technics in power electronics, so it is very important to study as a first step the application of model predictive control (MPC) in a current control scheme. The proposed predictive control strategy is based on the fact that only a finite number of possible switching states can be generated by a static power converter and that models of the system can be used to predict the behavior of the variables for each switching state [5]. This chapter presents a model predictive control (MPC) strategy to regulate the capacitor voltages and current of five and nine-level packed U cell inverters in stand-alone and grid connected mode and also applied MPC controller in two-level inverter to compare the simulation results with those obtained by PUC topology.

II.2. PUC 5 topology and switching sequences

Figure II.1 shows PUC5 inverter topology, which consists of six active switches, one isolated DC supply and one DC capacitor as second DC source (or dependent DC source), where each pair of switches (S_1&S_4, S_2&S_5 and S_3&S_6) is working complementarily. Figure II.1 shows also all the paths made by different switching states that have been studied noticing the effects on capacitor voltage as illustrated in Table II.1 [6].

The DC source and link amplitudes indicate the number of output voltage levels, use the ratio of 1/2 leads to generate a five-voltage level at the inverter output. So if V1 = *2V2* = 2E, then the output voltage (V_{ad}) contains the voltage levels of 0, ±E, ±2E. To reduce the number of isolated DC sources, an energy storage device (DC capacitor) is used at the second DC bus which needs voltage balancing methods such as linear/nonlinear controllers or the advance predictive control to fix the DC voltage accordingly [6]. The voltage control method is explained in details in next section.

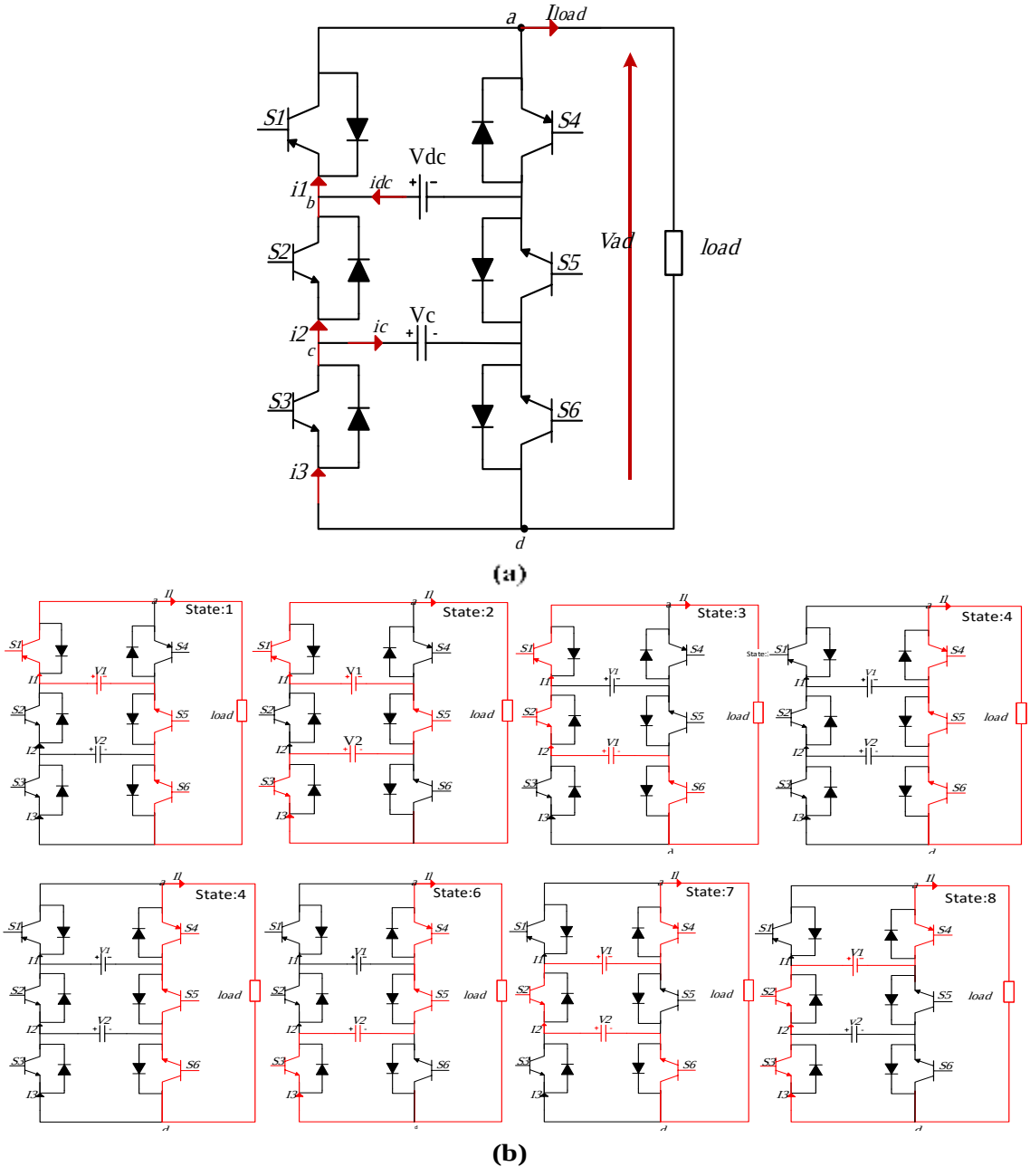


Figure II.1: (a) PUC5 Topology, (b) switching states of PUC 5 inverter

Table II.1: PUC5 capacitor voltage states

State	S1	S2	S3	Output voltage (Vad)	Capacitor voltage
0	1	0	0	V_{dc}	No effect
1	1	0	1	V_{dc} -V_c	Charging
2	1	1	0	V_c	Discharging
3	1	1	1	0	No effect
4	0	0	0	0	No effect
5	0	0	1	- V_c	Discharging
6	0	1	0	V_c - V_{dc}	Charging
7	0	1	1	- V_{dc}	No effect

II.3. Model predictive control of PUC 5

Different control methods for voltage balancing and current control exist such as linear/nonlinear controllers, predictive model, fuzzy, etc...[5]. Model Predictive Control or MPC is an advanced and effective strategy to control the power converters. It is based on the mathematical model of the studied system in order to predict the future behavior of the controlled variables. Then, to form these predictions, a cost function defined and evaluated in order to select the optimal control action [6]. One of the major advantages of the MPC compared to a traditional PI controller is the flexibility to control different variables, with limitations and additional system requirements. The defects of Model Predictive Control requires a high number of calculations to generate its output, compared to a classical continuous control scheme [6].

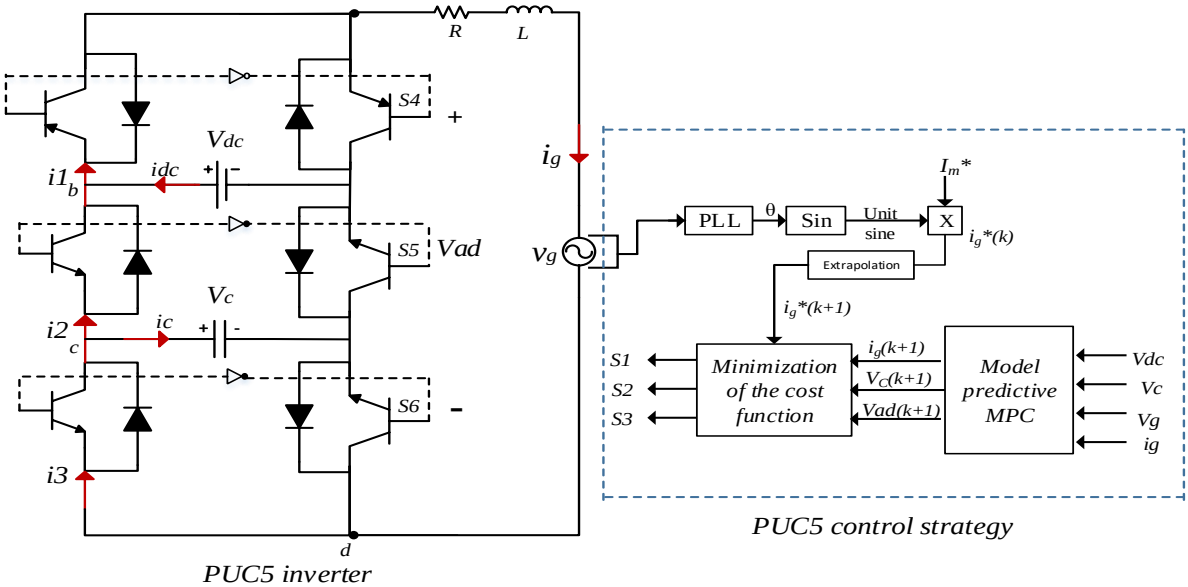


Figure II.2: Grid-connected PUC5 inverter with designed controller

Figure II.2 Presents the proposed control scheme based on model predictive (MPC) grid-connected PUC5 inverter. In which i_g is the injected current from inverter to the grid, the typical controller has been designed to control the amplitude and phase-shift of the grid current i_g results in delivering active power and exchanging reactive power desirably with the grid by the PUC5 inverter [1]. In the control strategy shown in Figure II.2, the grid voltage v_g is measured and sent to the PLL to extract its phase angle θ, and sent it to the Sin block. This unit sine wave is multiplied by desired value as maximum reference current I_{gmax}^* which can control the amount of power injected to the grid. Then the reference grid current i_g^* is extrapolated to calculate the future value of the reference current $i_g^*(k+1)$. The model predictive control consists of measuring the variables $V_c(k)$, $i_g(k)$ and the vector voltage $V_{ad}(k)$, and use it in the predictive control in order to calculate the future value $V_c(k+1)$, i_g $(k+1)$ and $V_{ad}(k+1)$ of the controlled variable for each one of the switching states. Then, a cost function is calculated in order to choose the minimum value corresponding to the optimal state and apply it on the PUC5 inverter through the switching pulses [6].

The switching functions of the PUC5 inverter shown in are defined as:

$$S_i = \begin{cases} 0 \text{ if } S_i \text{ OFF} \\ 1 \text{ if } S_i \text{ ON} \end{cases} \quad i = 1,2,3 \qquad \text{II.1}$$

The inverter output voltage can be formulated as:

$$V_{ad} = V_{ab} + V_{bc} + V_{cd} \qquad \text{II.2}$$

Where the points *a*, *b*, *c* and d are demonstrated in Figure II. 1 and each voltage can be computed based on the switching function as:

$$\begin{aligned} V_{ab} &= (S_1 - 1)V_1 \\ V_{bc} &= (1 - S_2)(V_1 - V_2) \\ V_{cd} &= (1 - S_3)V_2 \end{aligned} \qquad \text{II.3}$$

By substituting equation (II.3) into (II.2), then:

$$\begin{aligned} V_{ad} &= (S_1 - 1)V_1 + (1\text{-}S_2)(V_1\text{-}V_2) + (1\text{-}S_3)V_2 \\ V_{ad} &= (S_1 - S_2)V_1 + (S_2\text{-}S_3)V_2 \end{aligned} \qquad \text{II.4}$$

Since one of switches in each pair of S_1&S_4, S_2&S_5 and S_3&S_6 are turned ON, the switches current can be shown as a function of grid current and switching function:

$$\begin{aligned} i_1 &= S_1 i_g \\ i_2 &= S_2 i_g \\ i_3 &= S_3 i_g \end{aligned} \qquad \text{II.5}$$

Where

$$i_3 = i_c + i_2 \quad \text{II.6}$$

$$i_c = (S_3 - S_2) i_g \quad \text{II.7}$$

Concerning the capacitor voltage:

$$i_c = c \frac{dV_c}{dt} = (S_3 - S_2) i_g \quad \text{II.8}$$

$$\frac{dV_c}{dt} = \frac{(S_3 - S_2) i_g}{c} \quad \text{II.9}$$

Using the Euler Forward Approximation, the capacitor voltage can be replaced by equation:

$$\frac{dV_c}{dt} = \frac{V_c(k+1) - V(k)}{T_s} \quad \text{II.10}$$

Where, *Ts* is the sampling time.

Replacing (II.10) in (II.8), equation (II.9) can be obtained as the following:

$$V_c(k+1) = V_c(k) + \frac{T_s (S_3 - S_2)}{C} \times i_g \quad \text{II.11}$$

The grid current dynamics can be described by the vector differential equation (II.12) as:

$$V_{ad} = R \times i_g - L \frac{di_g}{dt} - v_g \quad \text{II.12}$$

Using again the Euler Forward Approximation, the grid current can be expressed by:

$$i_g(k+1) = (1 - \frac{T_s \times R}{L}) \times i_g + \frac{T_s}{L} (V_{ad}(k) - v_g) \quad \text{II.13}$$

Finally, the cost function *g* is derived as equation (II.14):

$$g(k) = \lambda_1 \left| i_g^*(k+1) - i_g(k+1) \right| + \lambda_2 \left| V_{dc} - 2V_c(k+1) \right| \quad \text{II.14}$$

The cost function *g* is calculated for the 8 possible switching states, and S_1, S_2, and S_3 are chosen for the minimum value of *g*, are then selected based on Table II.1 to be sent to the PUC inverter switches. λ_1 and λ_2 are two weighting factors, they are used to avoid coupling effects in case of using several variables in the cost function. Indeed, there are no analytical or numerical methods as such to adjust the weighting factors. In case of cost function where there is only one variable to be controlled, there is no need for weighting factors [6].

Figure II.3 exposed the flowchart of the proposed MPC applied on the 5-level PUC inverter. Two loops are executed. The outer loop, consisting of measuring the grid current i_g and the capacitor voltage V_c is executed every sampling time; while the inner loop is executed

for each possible state. The inner loop consists of calculating the predictive values of the grid current and the capacitor voltage and then calculating the cost function *g* in order to store the optimal values. After executing the 8 possible states, the minimum value of *g* is chosen and the corresponding switching states are applied to the semiconductor.

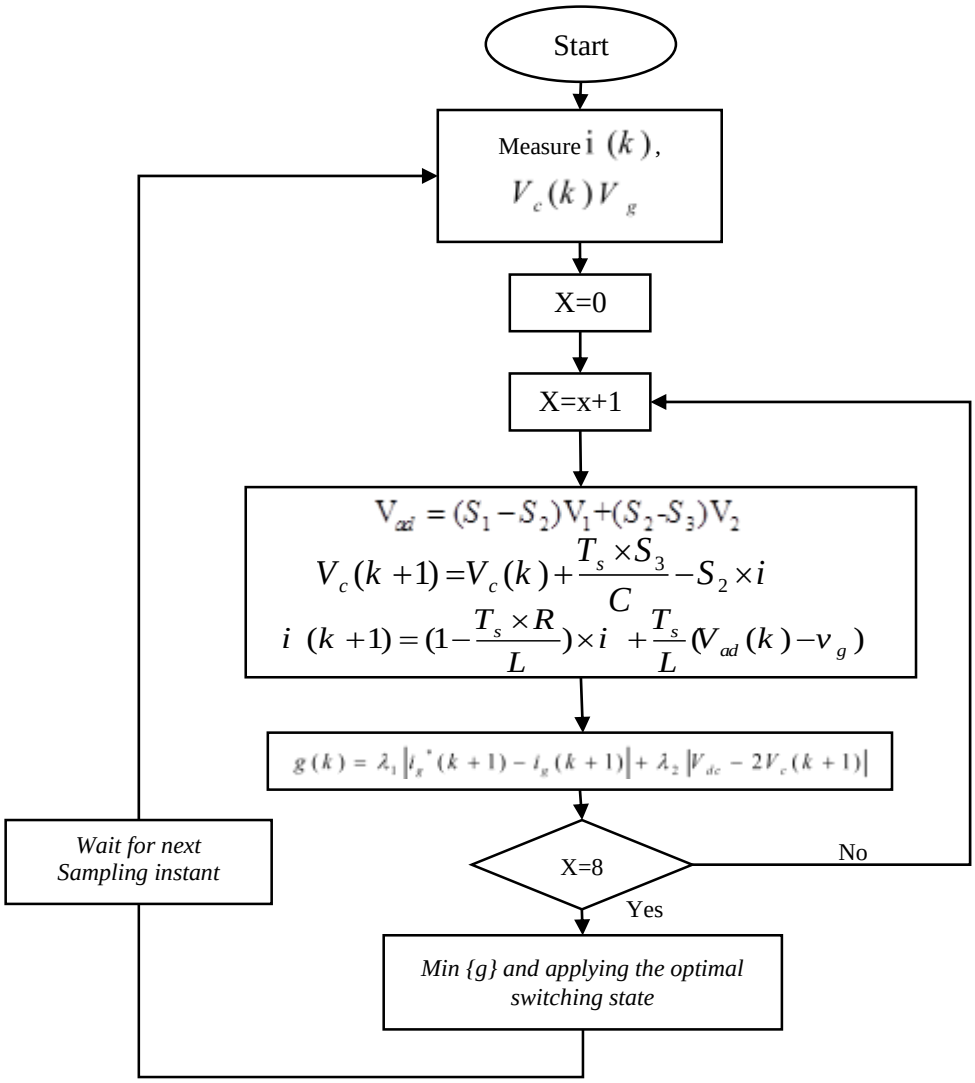


Figure II.3: Flowchart of the proposed MPC for PUC5

II.3.1. Simulation results

Numerous numerical simulations using Matlab/Simulink and sim-power systems packages of the proposed system are carried out. The PUC5 inverter has been tested in two different applications, stand-alone and grid connected modes. Simulation parameters have been illustrated in Table II.2. In order to verify the good performance of the proposed system, a comparison between the proposed MPC control technique and a conventional control technique

based on a PI controller and a PWM modulator has been accomplished as show in Table II.4

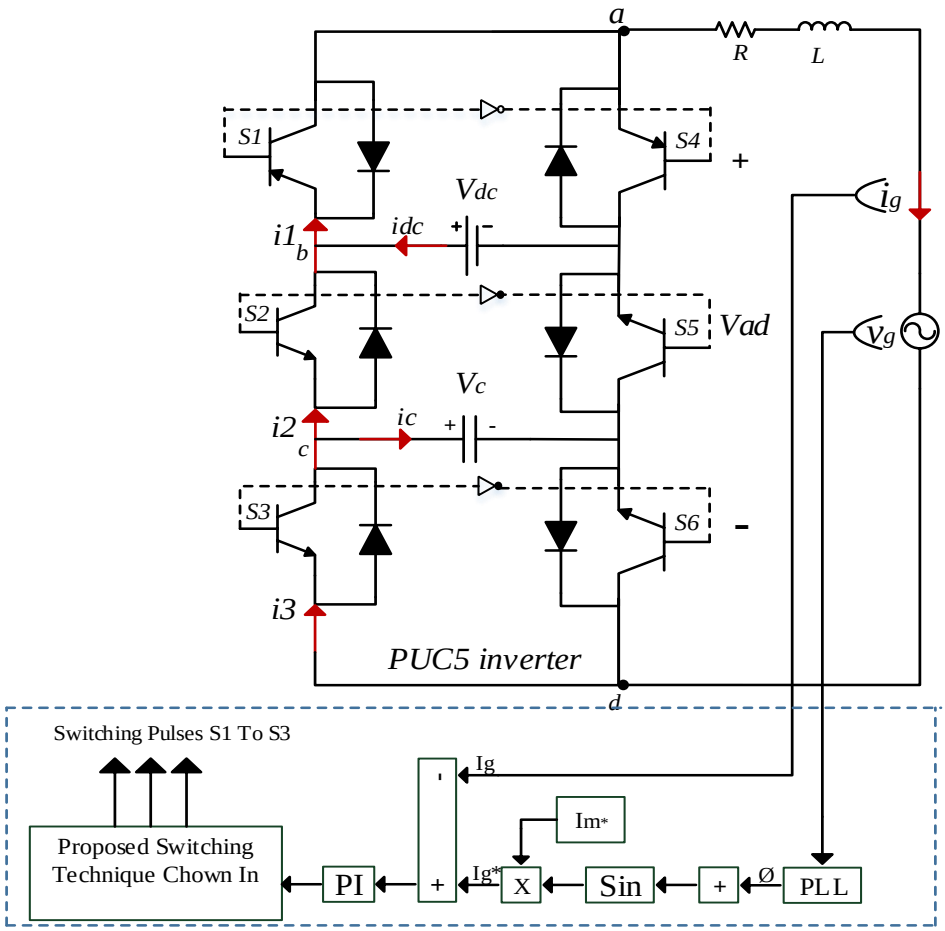


Figure II.4: Control scheme of the conventional control technique-based PI-PWM modulator For PUC5

Table II.2: Test parameters

Parameters	Value
Grid voltage v_g	150V
Grid frequency f	50 Hz
Grid side inductor *L*	5 mH
Grid side resistor *R*	0.1 Ω
DC capacitor *C*	2200 µF
Load side resistor *R*	30 Ω
Load side inductor *L*	20 mH

a) Test 1: Stand-Alone Mode

PUC5 inverter topology using conventional control strategy-based on PI regulator with PWM modulator presented in Figure II.4 has been tested under various current conditions and fixed load.

Figure II.5 shows the DC link capacitor voltage, load current and five-level output voltage waveforms under fixed load condition using the conventional control technique, as can be seen the DC link capacitor voltage is well regulated around half of the DC source voltage and show a good tracking of the desired reference voltage. On the other hand, the load current is well regulated around its reference with a quasi-sinusoidal form. Figure II.8 shows the THD analysis of the load current, where the obtained THD is less than 5%. Furthermore, a symmetrical 5-level waveform is well generated at the inverter output.

Furthermore, to show the dynamic performance of the conventional control technique, a variation in the load current reference is occurred. Figure II.6 presents the response of the system under current variation, where the obtained results show that the load current present a good tracking response of its reference and kept their sinusoidal form, otherwise, the DC link capacitor voltage shows a fluctuation of 5 volts around its reference as illustrated in Figure II.7.

PUC5 inverter topology using model predictive control strategy has been also tested under various current conditions and fixed load. Simulation results of this test under steady state condition are provided in Figure II.9. As shown in Figure II.9, the DC link capacitor voltage is well balanced at desired voltage reference and equal to the 1/2 of the DC source voltage, where the load current is regulated at the maximum value without any fluctuations and with perfect sinusoidal form. On the other hand a symmetrical five level voltages waveform has been perfectly generated at the PUC5 inverter output. The load current harmonic contents analysis presented in Figure II.12 show low amount of THD (<5%) and lesser than the obtained THD% with the conventional control strategy which prove the effectiveness of the proposed controller.

In order to verify the robustness of the proposed control technique, a variation in the load current reference is applied on the proposed system. The obtained results presented in Figure II.10 prove the good dynamic performance of MPC in variable reference current conditions in terms of load current waveform and DC link voltage response as illustrated in Figure II.11, where the DC link voltage shows a very small fluctuation compared to the obtained response using the conventional control strategy. Table II.3 illustrates a comparison summary table between the obtained results between the proposed system using MPC and the

conventional control technique based on PI with PWM in terms of current quality and DC link capacitor voltage fluctuations.

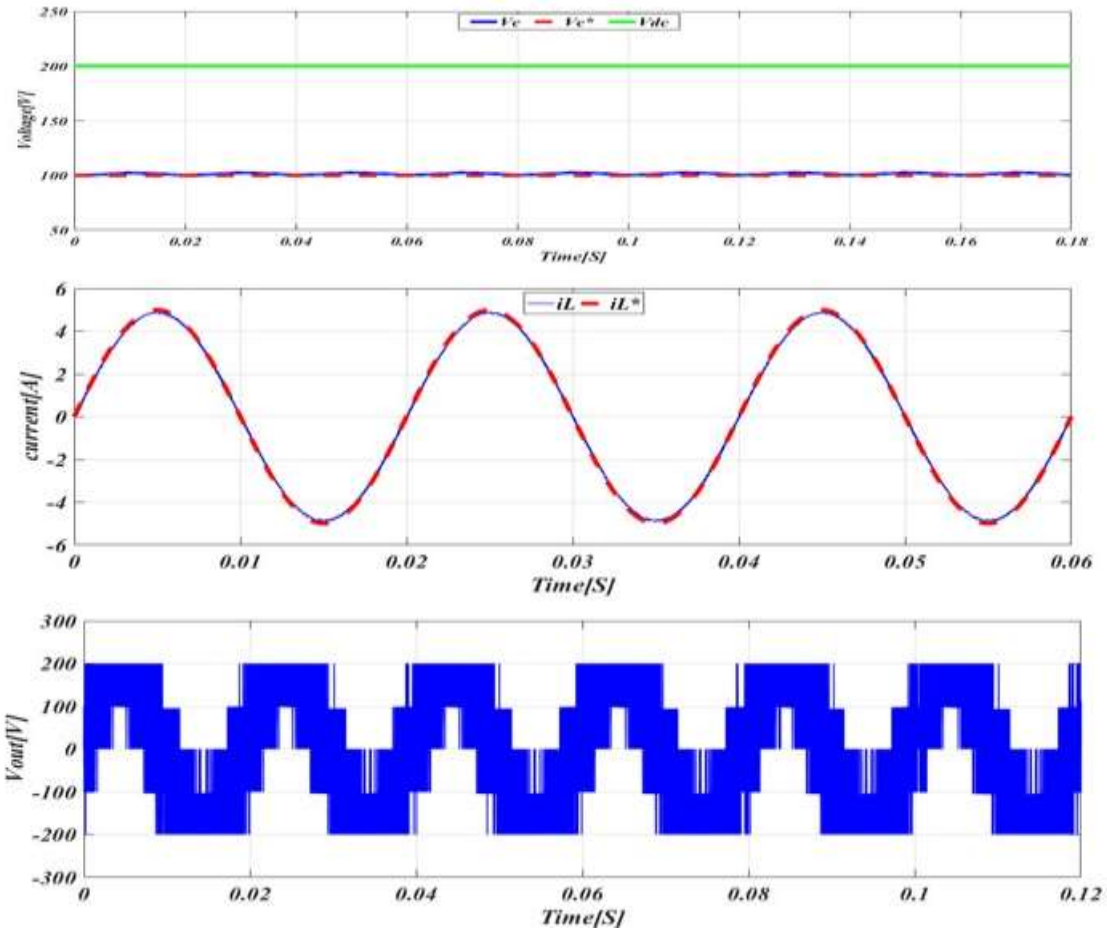


Figure II.5: Simulation results of PUC5 using PI with PWM

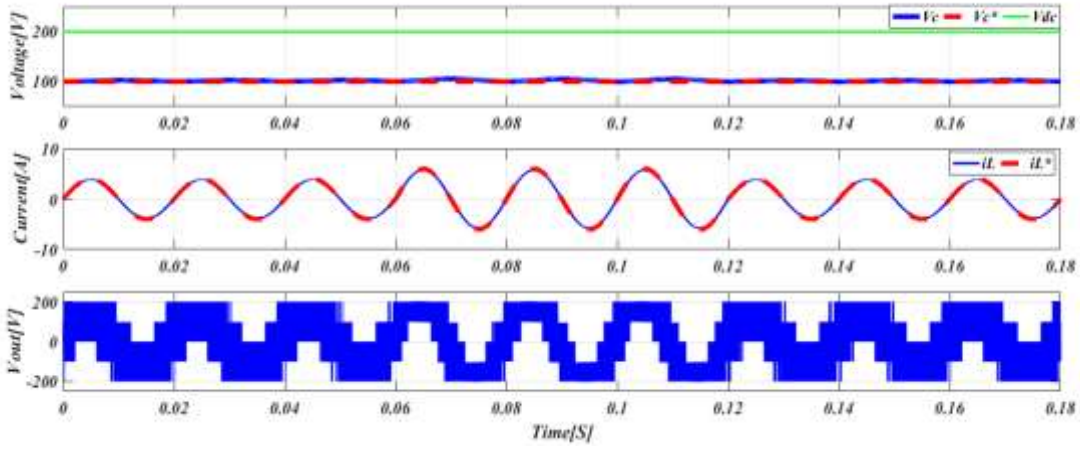


Figure II.6: Response of DC link capacitor voltage, load current and five-level output voltage, under current variation using PI with PWM

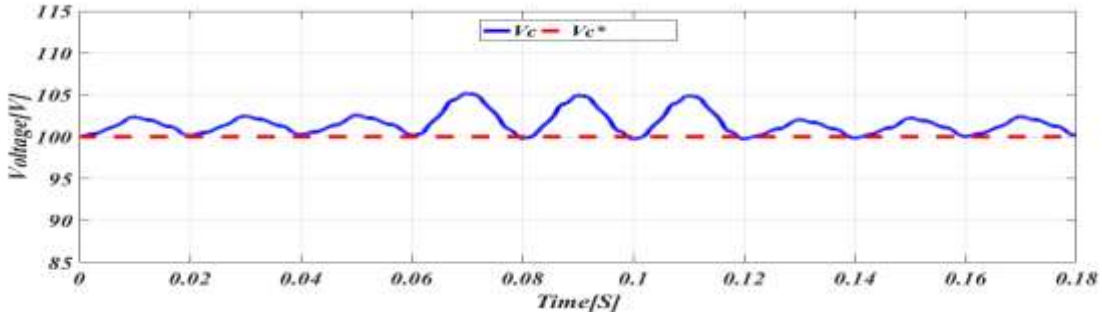


Figure II.7: Zoom of the DC link capacitor voltage variation using PI with PWM

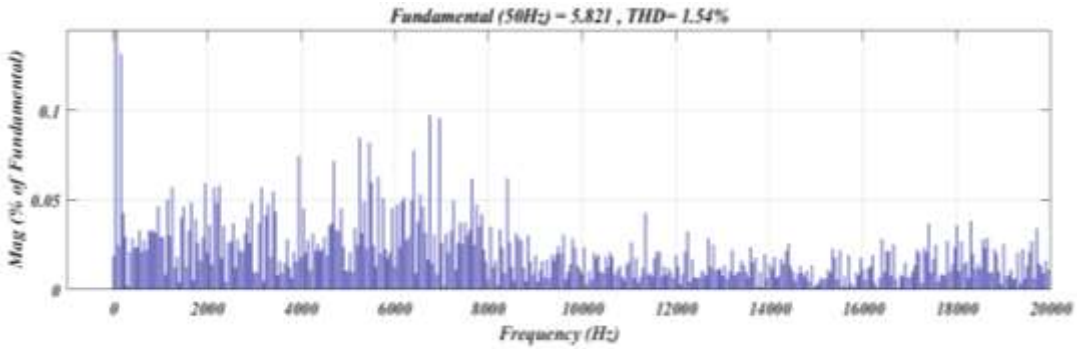


Figure II.8: THD analysis of load current using PI with PWM

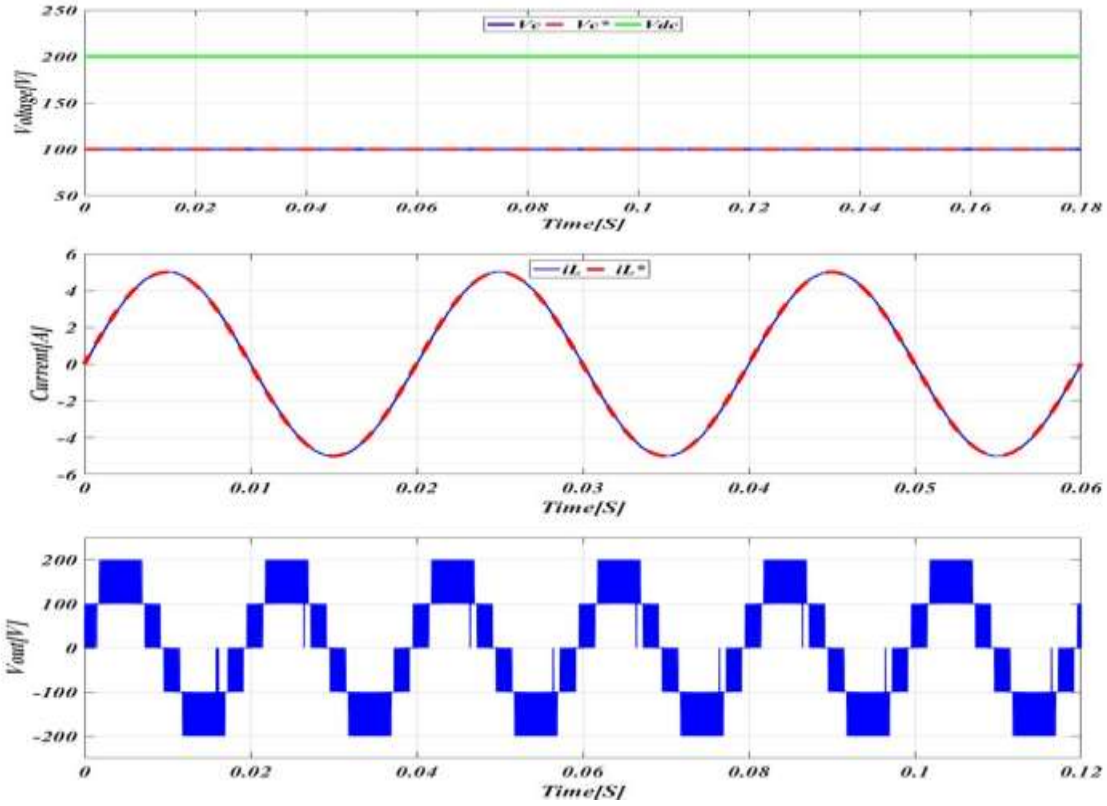


Figure II.9: Simulation results of PUC5 operation under fixed load condition using MPC

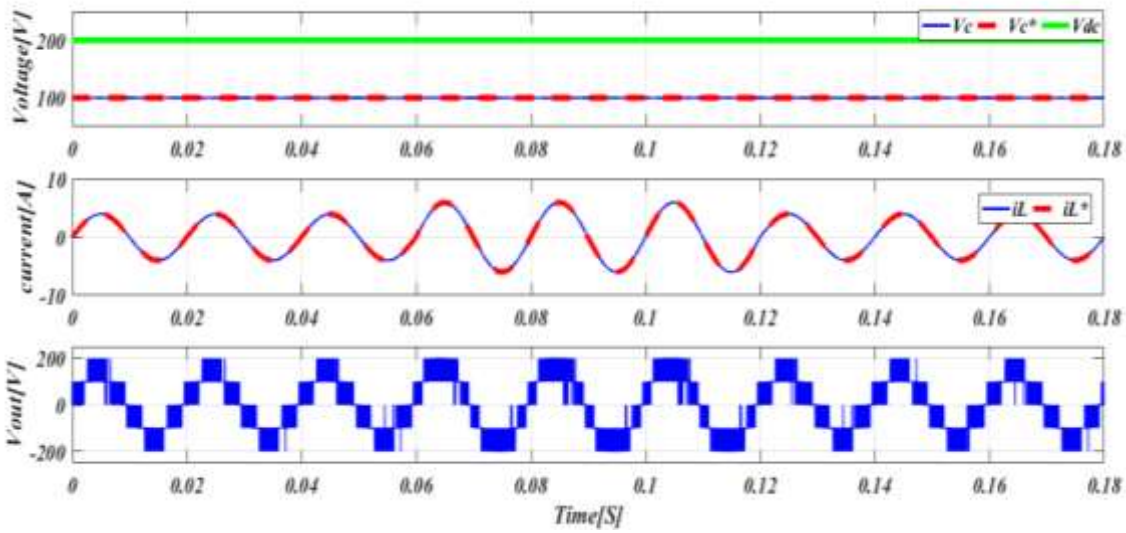


Figure II.10: Response of capacitors voltage, load current and five-level output voltage under current variation using MPC

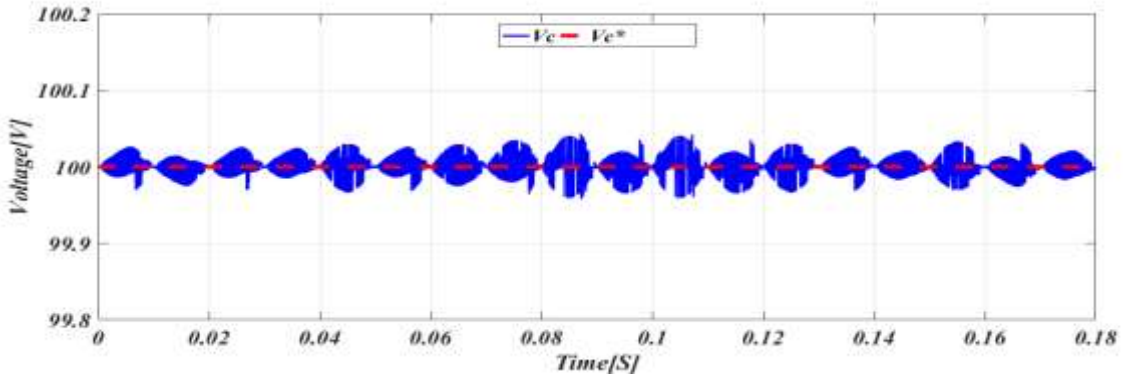


Figure II.11: Zoom of the DC link capacitor voltage using MPC

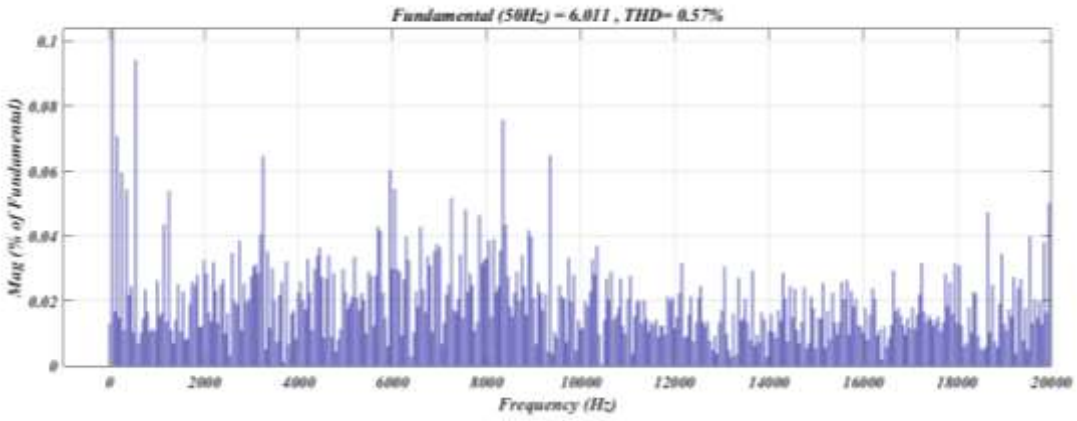


Figure II.12: THD analysis of load current

Table II.3: Comparison between PI with PWM and MPC

	THDi (%)	Voltage variations in the capacitor's (V)
Regulator PI with PWM	1.54	5.25
Controller MPC	0.57	0.06

b) Test 2: Grid-connected Mode

In this test, the PUC5 inverter is connected to a single-phase AC source where the proposed system aims to inject active power to the grid.

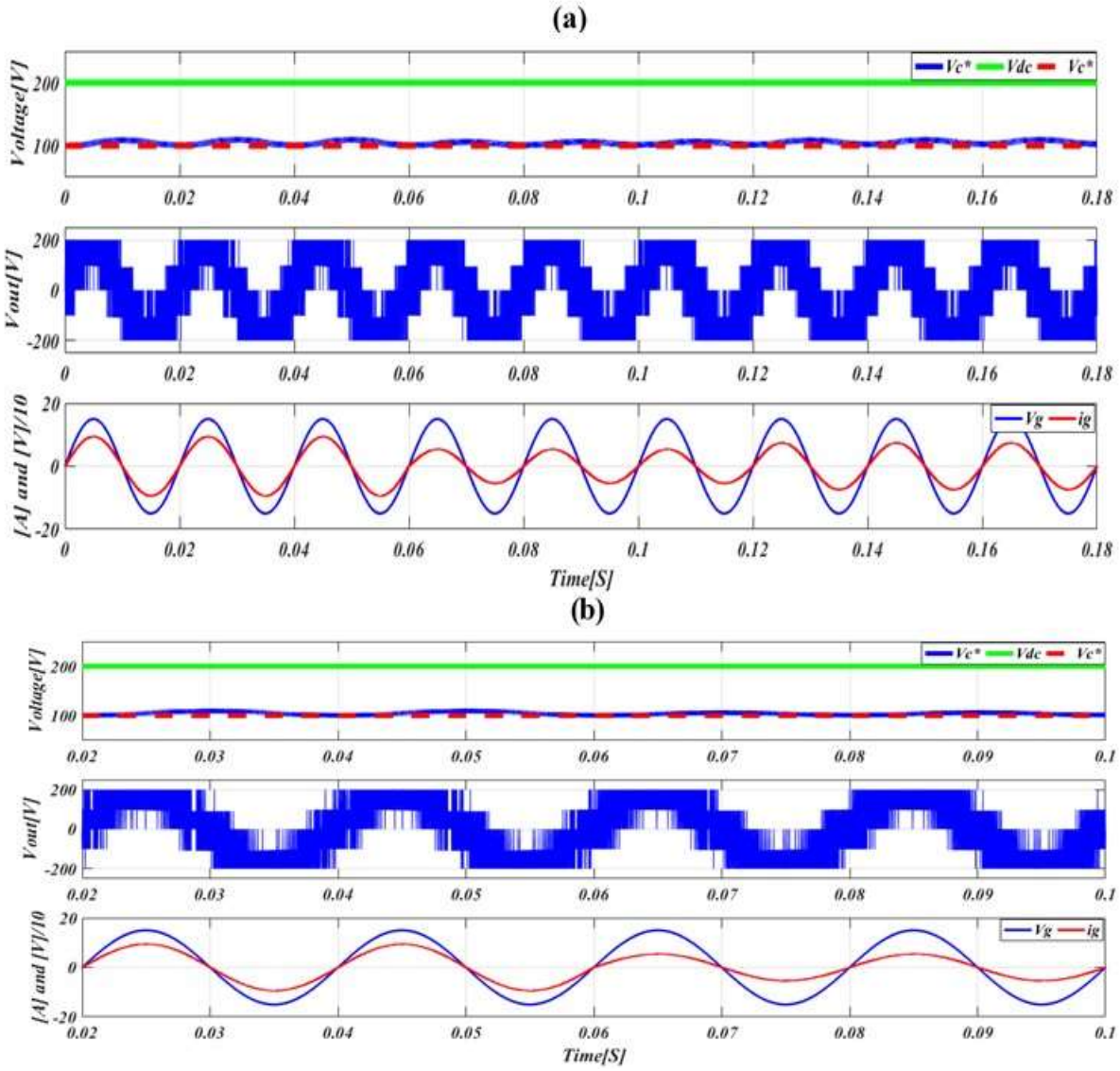


Figure II.13: Waveforms of DC link capacitor voltage, five level output voltage and grid current and voltage: (a) under grid current reference variation, (b) under fixed grid current reference using PI with PWM

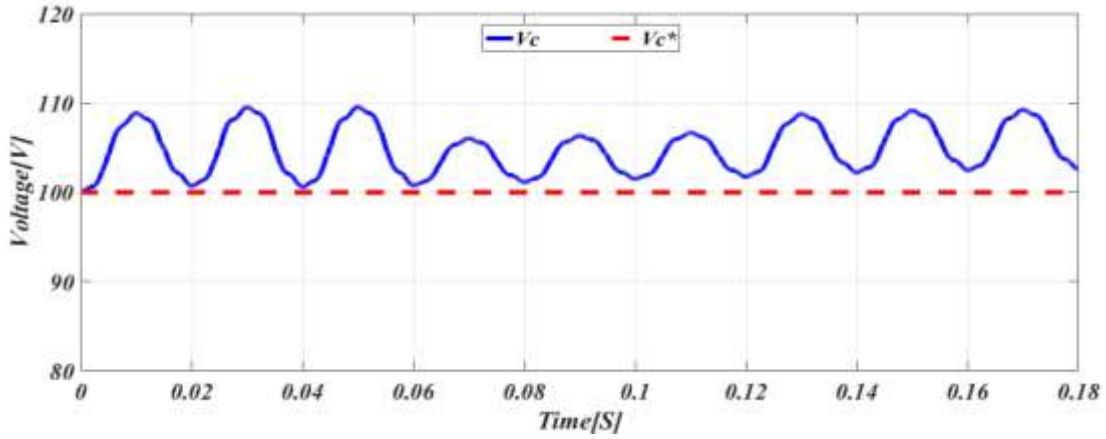


Figure II.14: Zoom of DC link capacitor voltage using PI with PWM

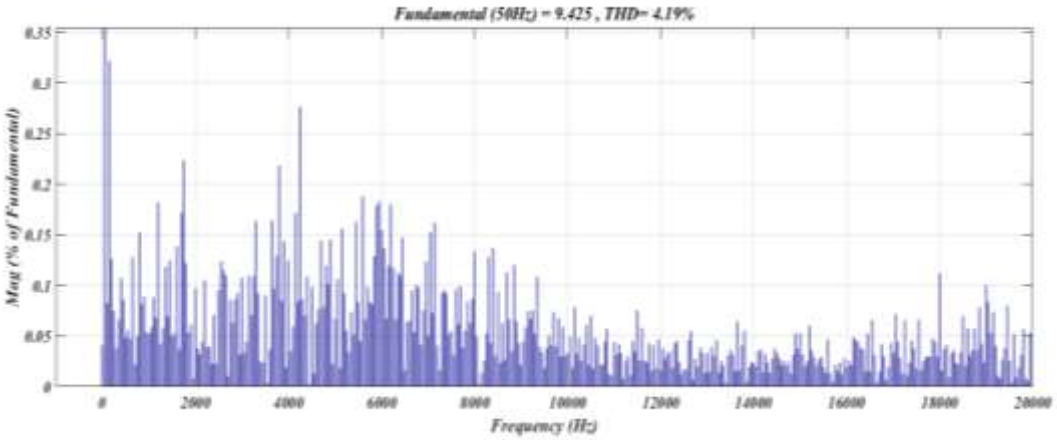


Figure II.15: THD analysis of the grid current

Figure II.13 (a) & (b) illustrates the dynamic and steady state response of the proposed PUC5 topology using conventional PI with PWM control strategy, as we can observed, the DC link capacitor voltage is oscillating around the reference value equal to half the DC source voltage and shows a voltage variation around the reference equal to 10 voltage as depicted in Figure II.14. On the other hand, the grid current has a good sinusoidal form and well synchronized with grid voltage under fixed and variable grid current reference with an THD less than 5% equal to 4.19% as presented in Figure II.15. Furthermore, the PI with PWM control strategy allows producing a five-level voltage waveform at the inverter output.

Figure II.16 (a) & (b) presents the response of the grid connected PUC5 topology using MPC, as presented the DC link capacitor voltage is well balanced around 1/2 of the DC source voltage and track perfectly its voltage reference allowing to produce a symmetrical five level voltage at the inverter output. On the other hand, the grid current has a perfect sinusoidal form

and perfectly synchronized with the grid voltage compared to the obtained results using the PI with PWM strategy.

In terms of DC link voltage fluctuations, the proposed system using MPC shows a very small voltage fluctuations less than 0.1 volt, as presented in Figure II.17. On other hand, the low amount of the grid current THD presented in Figure II.18 reveal the fact that the proposed MPC allows the system to perform at higher level of power factor (unity power factor).

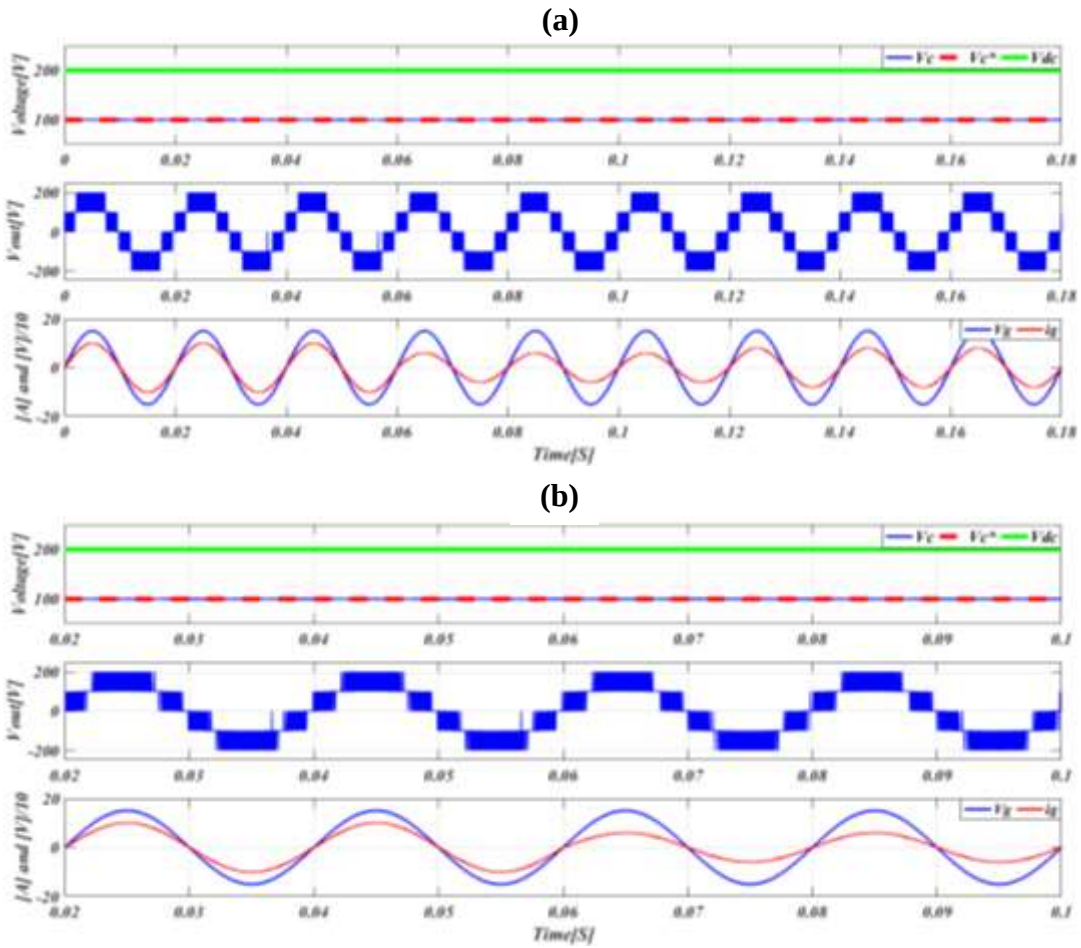
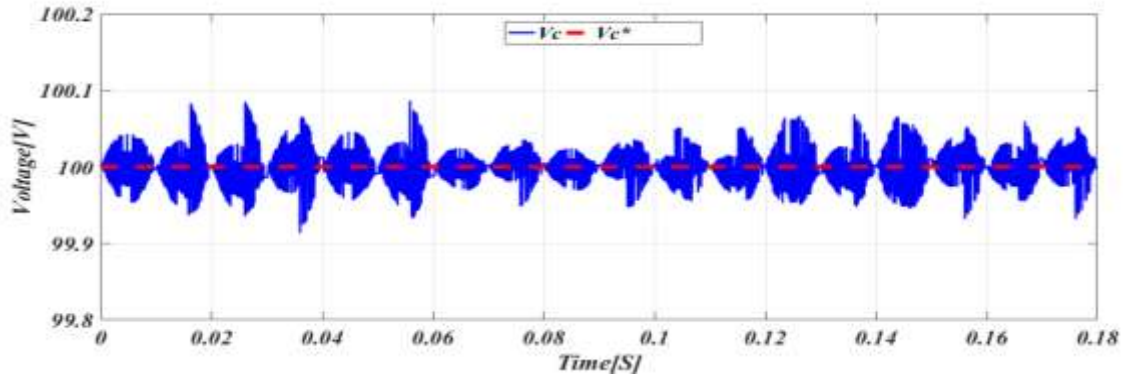


Figure II.16: Waveforms of DC link capacitor voltage, five level output voltage and grid current and voltage: (a) under grid current reference variation, (b) under fixed grid current



reference using MPC

Figure II.17: Zoom of DC link capacitor voltage using MPC

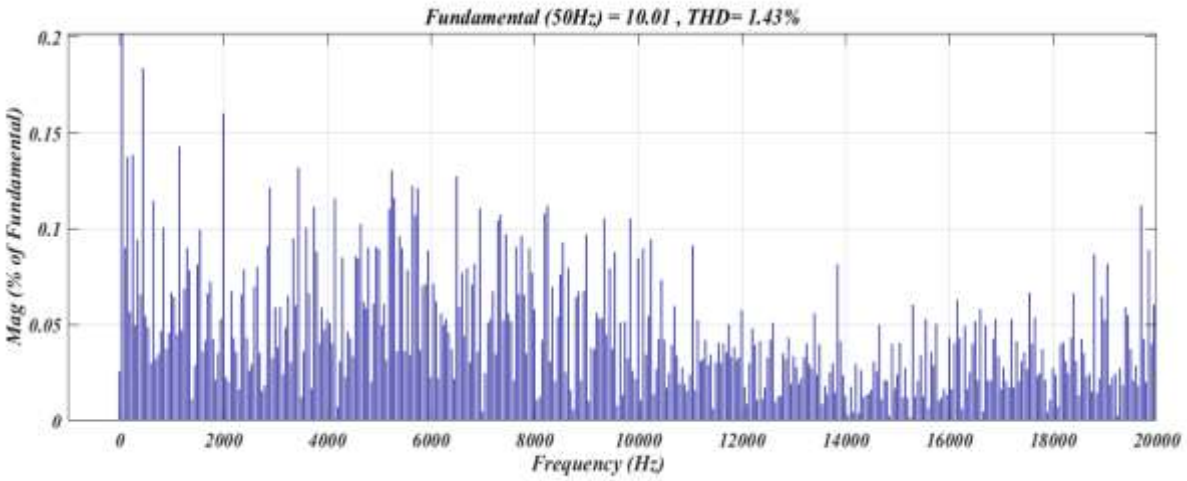


Figure II.18: THD analysis of the grid current

Table II.4: Comparison between PI with PWM and MPC

	THDi (%)	DC link capacitor voltage fluctuations (V)
Regulator PI with PWM	4.19	9.7
Controller MPC	1.43	0.07

II.4. PUC 9 topology and switching sequences

As shown in **Figure** II.19, nine-level PUC inverter is designed by adding another U-cell to PUC5 topology. It is composed of eight active switches, two capacitors and a single DC source. The power switches are organized into four pairs including (S_1, S_5), (S_2, S_6), (S_3, S_7) and (S_4, S_8) where they operate complementary to prevent the short circuit action. The first capacitor is called $C1$ and is charged to half of DC source; the other capacitor named $C2$ is also charged to one-fourth of DC source. Using the capacitors voltages and switching vectors presented in Table II.5, the nine-level voltage is generated at the inverter output.

As presented in Table II.5, the capacitor voltages charging and discharging in PUC9 are directly affected by the switching states. To achieve a balanced capacitors voltage, it is necessary to implement the PUC9 inverter under supervision of a closed loop control [7].

Table II.5: PUC9 Switching states and capacitor voltage charging and discharging modes.

state	S_1	S_2	S_3	S_4	Out voltage(Vad)	Capacitor voltage C1	Capacitor voltage C2

1	1	0	0	0	V_{dc}	No effect	No effect
2	1	0	1	0	V_{dc} - V_{c1}+ V_{c2}	Charging	Discharging
3	1	0	0	1	V_{dc} - V_{c2}	No effect	Charging
4	1	0	1	1	V_{dc} - V_{c1}	Charging	No effect
5	1	1	0	0	Vc1	Discharging	No effect
6	1	1	1	0	V_{c2}	No effect	Discharging
7	1	1	0	1	V_{c1}- V_{c2}	Discharging	Charging
8	1	1	1	1	0	No effect	No effect
9	0	0	0	0	0	No effect	No effect
10	0	0	1	0	V_{c2}- V_{c1}	Discharging	Charging
11	0	0	0	1	- V_{c2}	No effect	Discharging
12	0	0	1	1	- V_{c1}	Discharging	No effect
13	0	1	0	0	V_{c1}- V_{dc}	Charging	No effect
14	0	1	1	0	- V_{dc} + V_{c2}	No effect	Charging
15	0	1	0	1	V_{dc} + V_{c1}- V_{c2}	Charging	Discharging
16	0	1	1	1	- V_{dc}	No effect	No effect

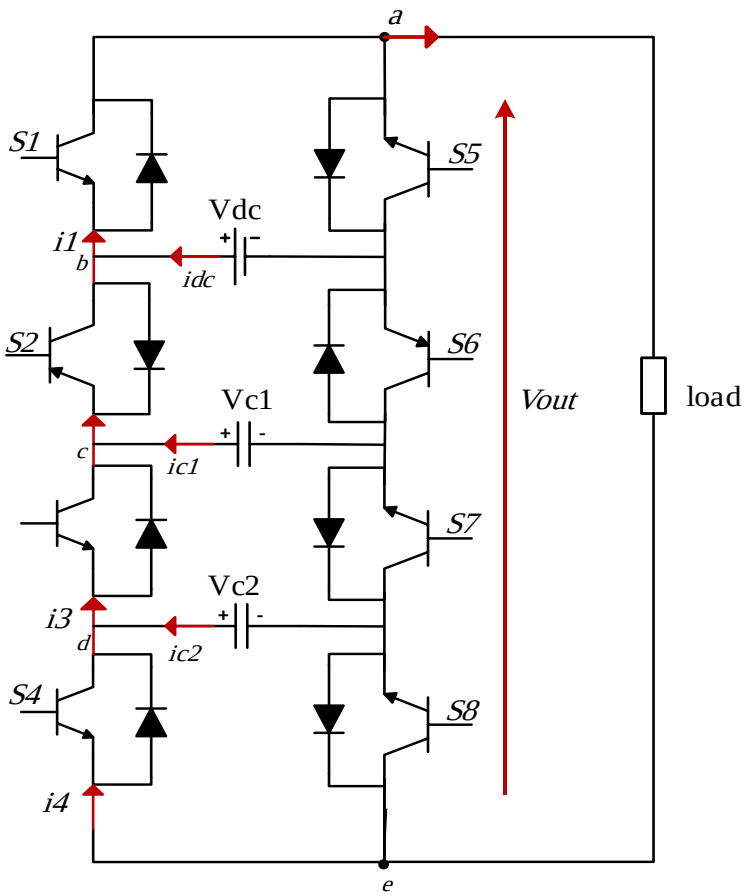


Figure II.19: Nine-level PUC inverter topology

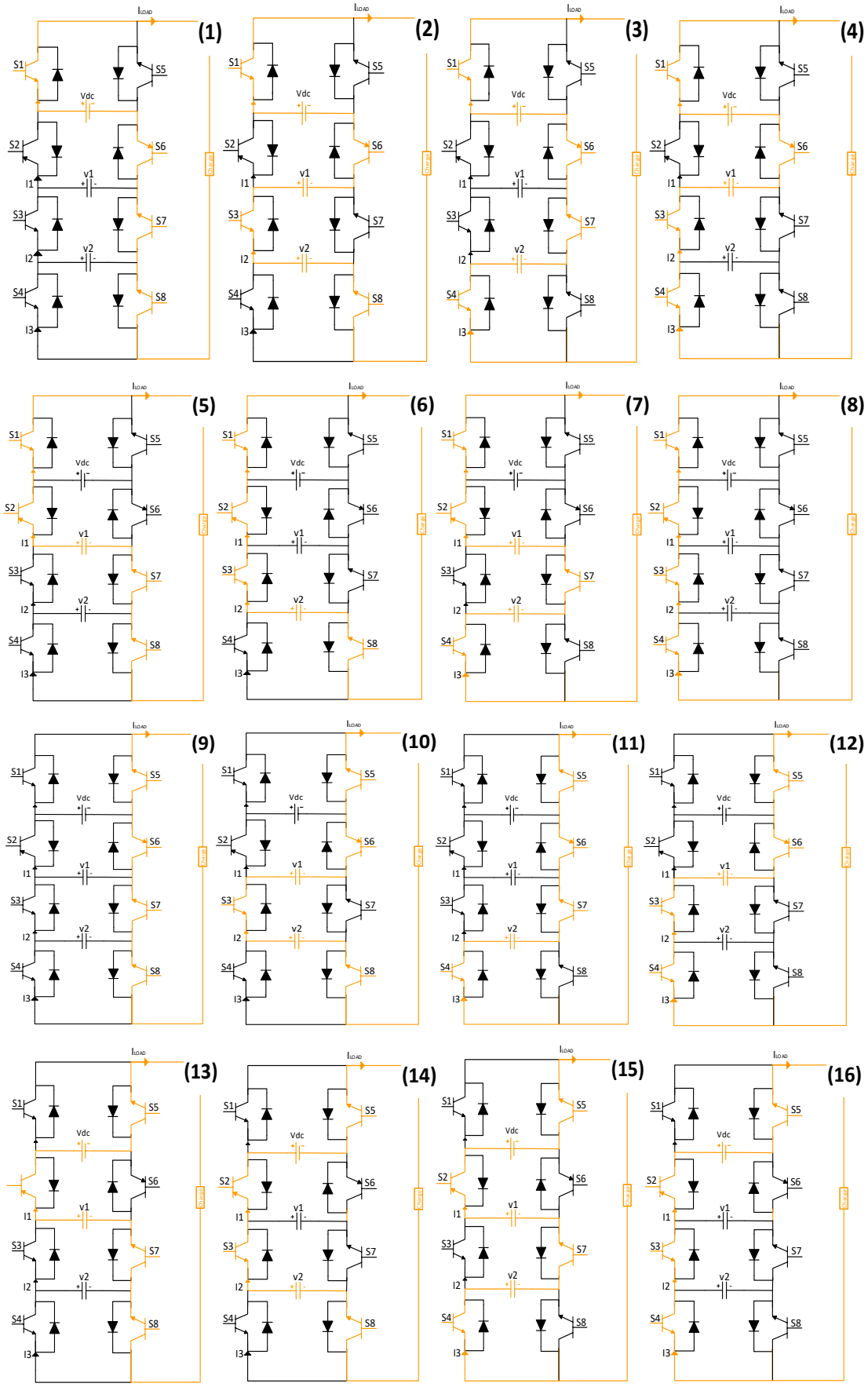


Figure II.20: Equivalent circuits of nine-level PUC in each switching state according to Table II.5

II.5. Model predictive control of PUC 9

Model predictive control is a discrete dynamic model-based controller, which selects the best switching vector through a cost function which can be defined based on mathematical models of PUC parameters like capacitors voltage, load current, switching frequency, switching modulator, …etc. One of the major advantages of MPC is direct selection of switching state without any switching modulator like SPWM or SVPWM, which reduces the cost and complexity of control loop design. In addition, due to exact modeling of PUC, which is used for MPC, the capacitors size can be decreased remarkably [9].

In this case, three variables are controlled by the proposed model predictive (MPC), which are the grid current i_g and the capacitors voltages V_{c1} and V_{c2}. The value of capacitor voltages V_{c1} and V_{c2} are regulated to $V_{dc}/2$ and $V_{dc}/4$ respectively in order to generate nine voltage levels. Figure II.21 presents the block diagram of MPC for nine-level PUC in grid-connected mode. For a stand-alone mode, the grid source will be removed from the control loop presented in Figure II.21.

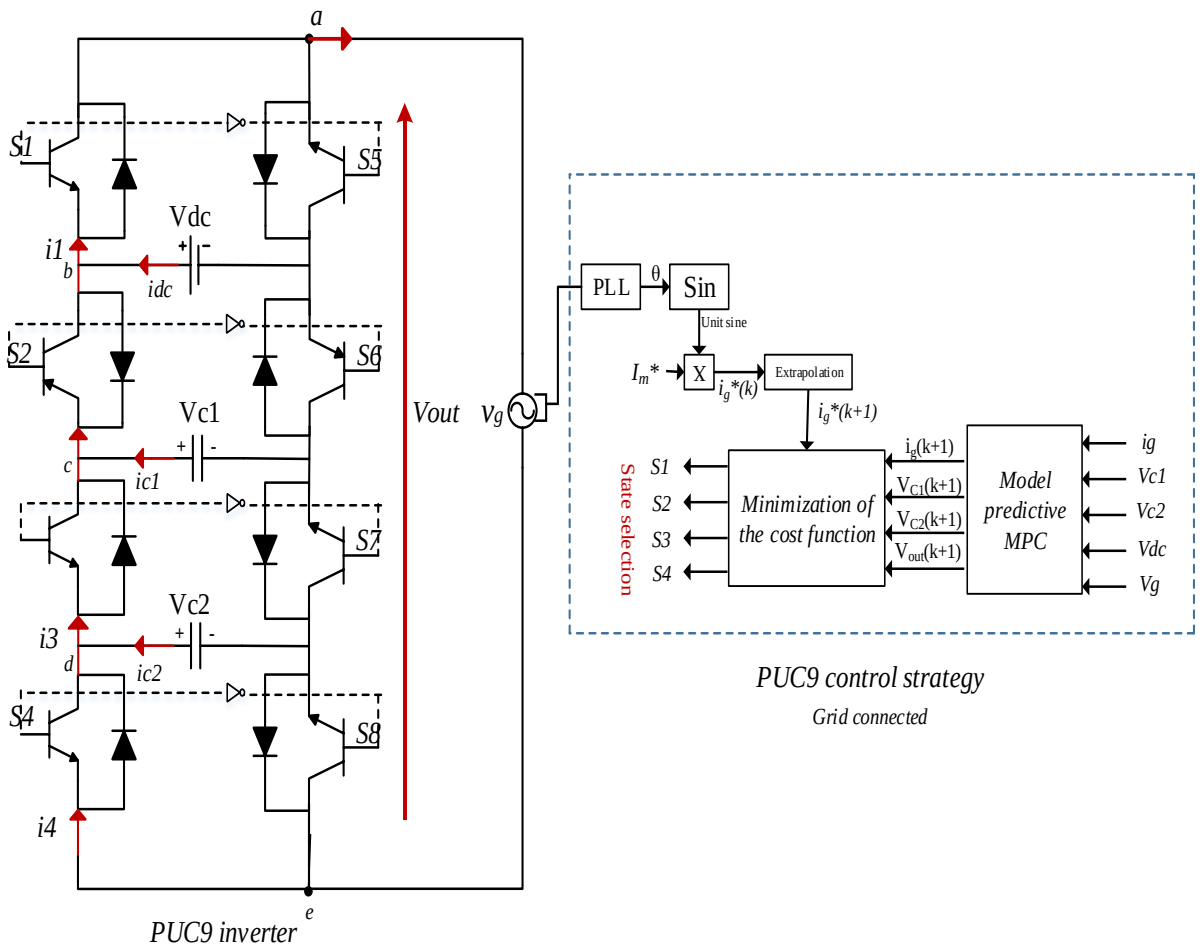


Figure II.21: Grid-connected PUC9 inverter with MPC controller

The grid-connected PUC9 inverter can be modelled using the Kirchhoff laws as follows:

$$L\frac{di_g(t)}{dt} = R \times i_g - V_{out} - V_g \quad \text{II.15}$$

$$C_2\frac{dVc_1(t)}{dt} = (S3 - S2)i_g \quad \text{II.16}$$

$$C_2\frac{dVc_2(t)}{dt} = (S4 - S3)i_g \quad \text{II.17}$$

Using again the Euler Forward Approximation, the capacitors voltage C_1, C_2 and the grid current can be expressed as:

$$i_g(k+1) = (1 - \frac{R \times T_s}{L})i_g + \frac{T_s}{L}(V_o(k+1) - V_g) \quad \text{II.18}$$

$$Vc_1(k+1) = Vc_1(k) + \frac{T_s}{C_1}(S_3 - S_2)i_g(k) \quad \text{II.19}$$

$$Vc_2(k+1) = Vc_2(k) + \frac{T_s}{C_2}(S_4 - S_3)i_g(k) \quad \text{II.20}$$

Where $i_g(k+1)$, $V_{c1,\,2}(k+1)$ are predicted models for load current and capacitors voltage for the next sample time respectively.

According to the predicted equations presented in Equations (II.18), (II.19) and. (II.20), the MPC cost function is defined as follows:

$$g(k) = \lambda_1\left|i_g^*(k+1) - i_g(k+1)\right| + \lambda_2\left|V_{c1}^* - V_c(k+1)\right| + \lambda_3\left|V_{c2}^* - V_c(k+1)\right| \quad \text{II.21}$$

Where $i_g^*(k+1)$, V_{c1}^*, V_{c2}^* are the desired values for the grid current and capacitor voltages respectively and λ1, λ2, λ3 are the cost function weighting factors, which are used to assign the importance of each term in the control process. The cost function weighting factors must be selected properly, they have direct effect on the MPC performance.

Figure II.22 shows a flowchart that explains the algorithm operation principle. The cost function g (k) is calculated for 16 possible switching states of Table II.5 in each sampling time. It selects the best switching state of the inverter.

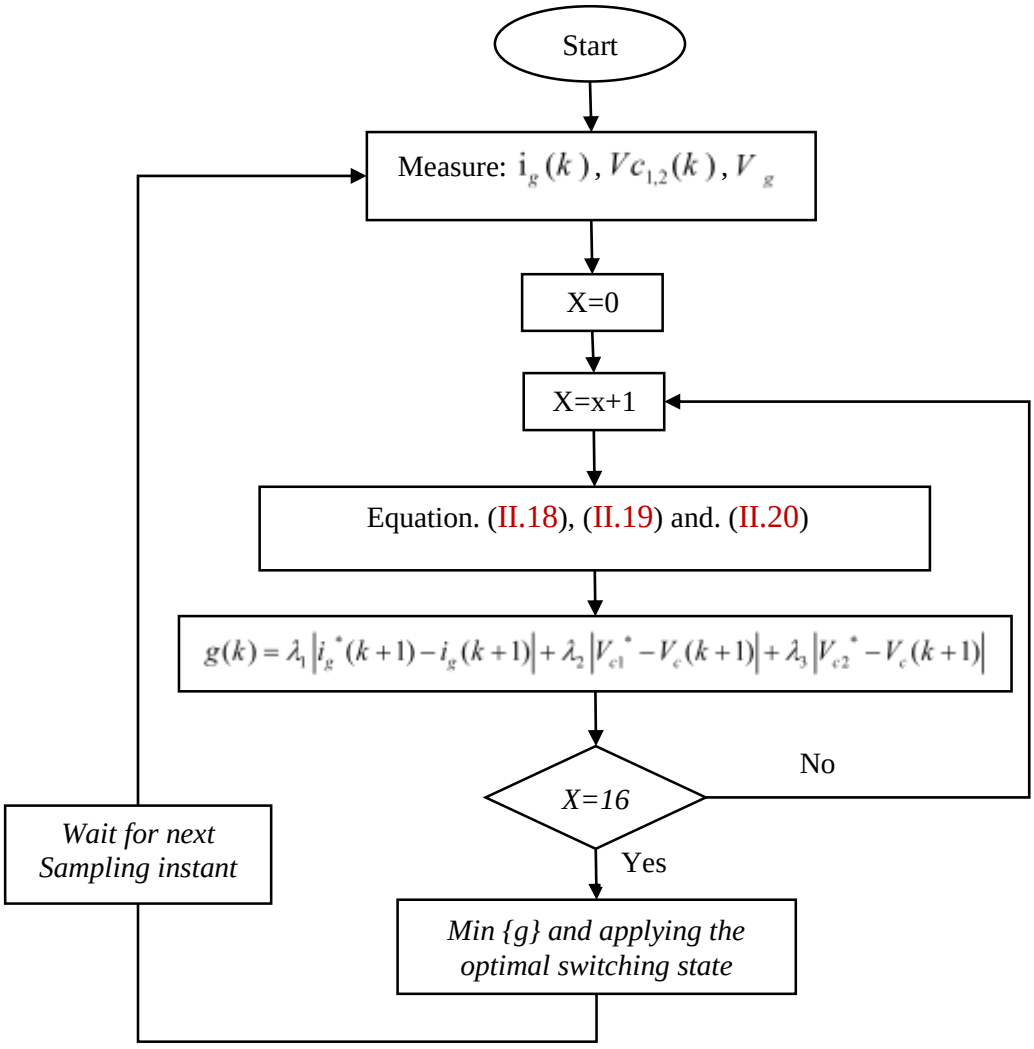


Figure II.22: Flowchart of the proposed MPC for PUC9

II.5.1. Simulation results

The proposed system has been exposed to several numerical simulations using Matlab/Simulink and sim-power systems packages. The PUC9 inverter has been also tested in both stand-alone and grid-connected applications. Simulation parameters are shown in Table II.2. A comparison between the proposed MPC control approach and a classic control technique based on a PI controller and a PWM modulator has been also carried out in order to validate the good performance of the proposed system using the nine-level inverter in terms of current THD and DC link voltage fluctuations.

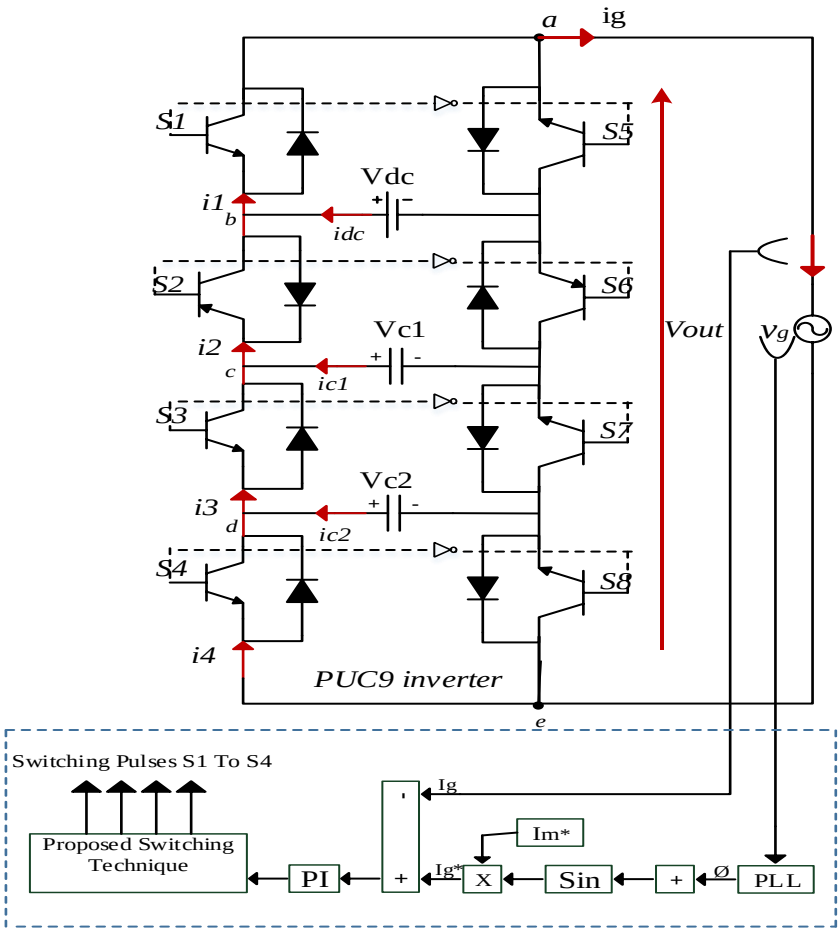


Figure II.23: Control scheme of nine-level inverter using the conventional control technique based on PI regulator with PWM modulator

a) Test 1: Stand-Alone Mode

Under various current conditions and fixed load, the PUC9 inverter topology has been tested using conventional PI with PWM and model predictive control strategies.

Figure II.24 shows the DC link capacitor voltages, load current and nine-level output voltage waveforms under fixed load condition using the conventional control technique-based on a PI controller and a PWM modulator, one can see that the DC link capacitors voltage are charged and well-regulated around their references, half and quarter of the DC source voltage for Vc1 and Vc2 respectively allowing to produce a perfect nine level voltage waveform at the inverter output. The load current has a quasi-sinusoidal form with a total harmonic distortion less than 1% as depicted in Figure II.27.

Figure II.25 illustrates the dynamic performance of the proposed topology using conventional control strategy under current reference variations, the DC link capacitors voltage shows a good balancing around their references and shows a small voltage fluctuations less than 1 volt (Figure II.26), where the load current kept the sinusoidal form along with the load

current reference variations. The inverter output voltage has always a perfect and symmetrical nine level voltage despite the current reference variations.

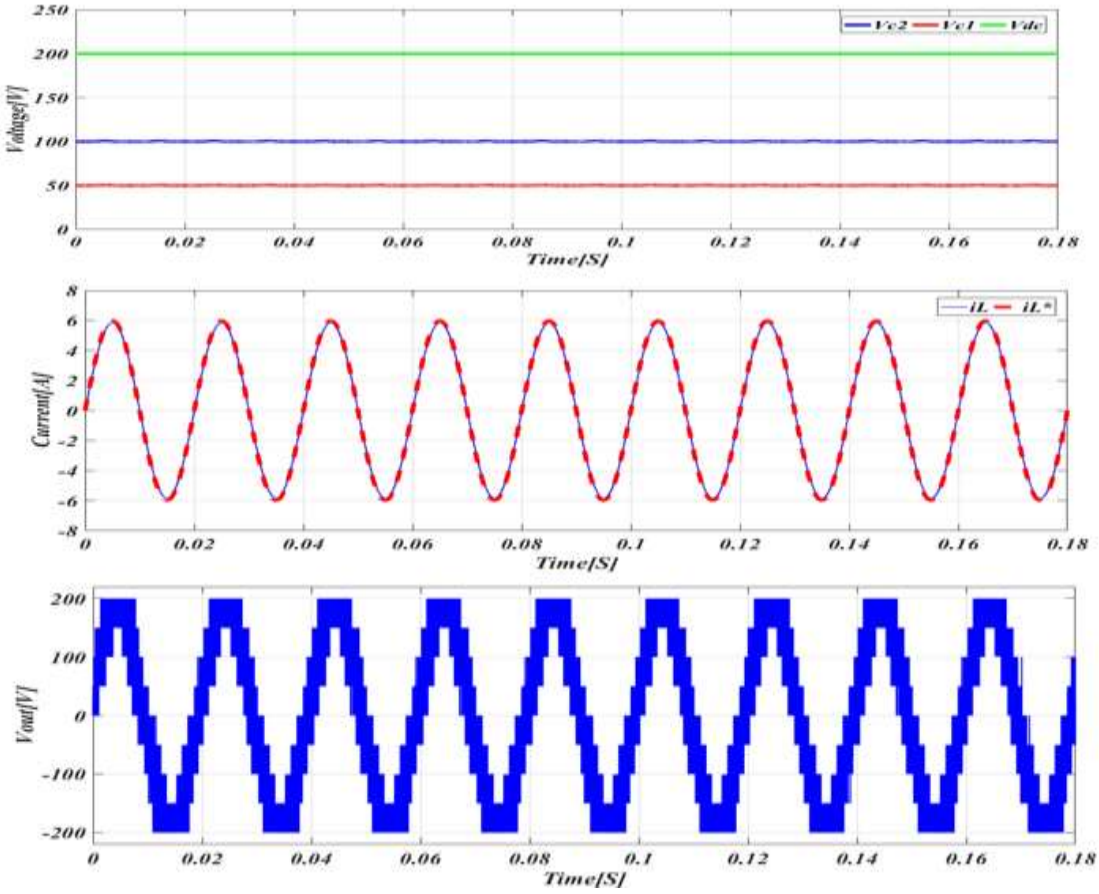


Figure II.24: Simulation results of PUC9 operation under fixed load condition using PI with PWM

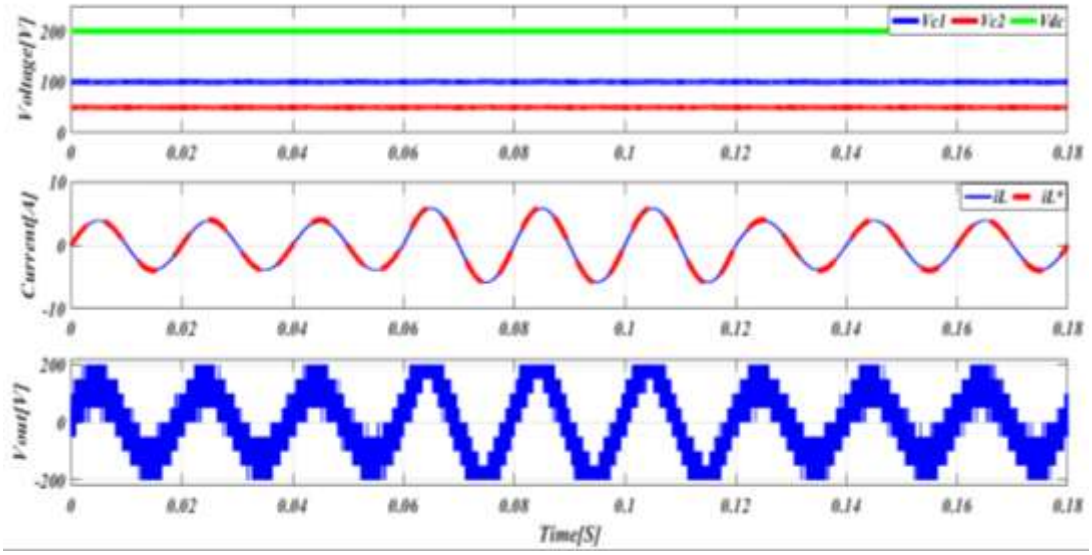


Figure II.25: Waveforms of capacitors voltage, load current and five-level output voltage under current variation using PI with PWM

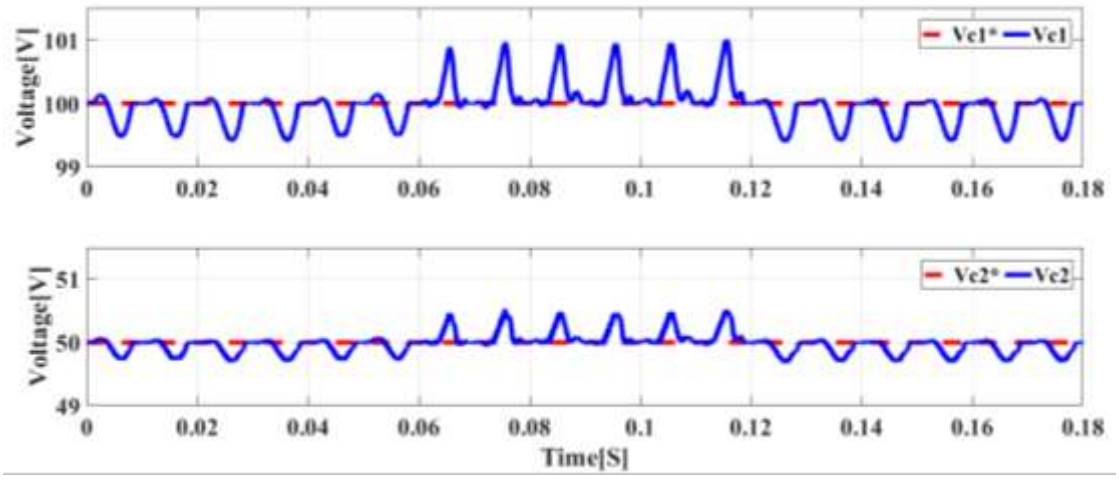


Figure II.26: Zoom of the DC link capacitors voltage using PI with PWM

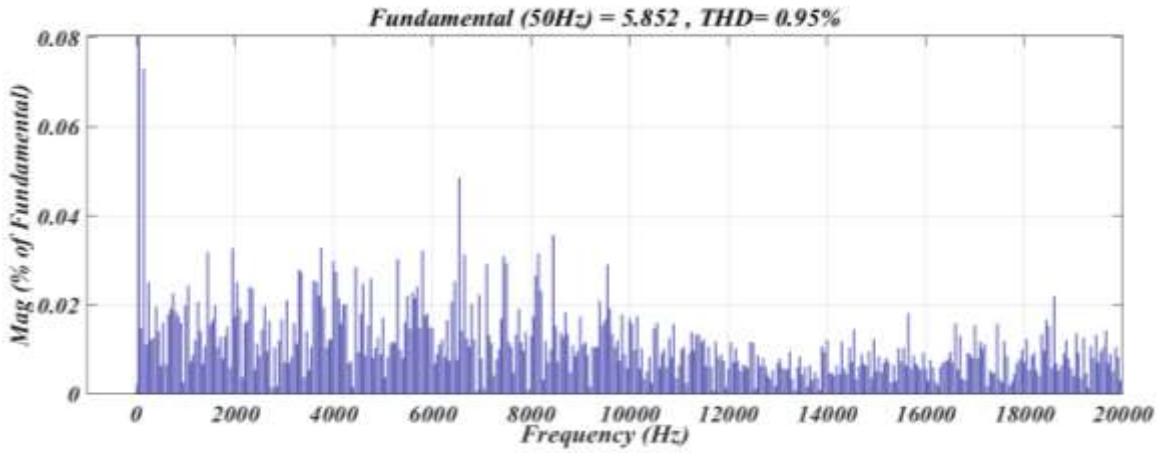


Figure II.27: THD analysis of load current

Figure II.28 & II.29 shows the simulation results of proposed topology using MPC control strategy this test under fixed load and variable load current reference conditions. As shown in Figure II.28 both capacitors are balanced at desired voltage reference, where Vc1 is equal to 1/2 of the DC source voltage and V_{c2} is equal 1/4 to the DC source capacitor. On the other hand the load current is regulated at the maximum value without any fluctuations and with perfect sinusoidal form. Furthermore, a symmetrical nine level voltages waveform has been perfectly generated at the PUC9 inverter output. The harmonic contents analysis of load current shown in Figure II.31 shows a low amount of THD (<5%) which prove the effectiveness of the proposed controller and better than the obtained THD using the conventional control strategy.

A variation in the load current reference has been applied to the proposed system in order to evaluate the dynamic performance of the proposed control technique. Figure II.29 shows the simulation results of load current and capacitors voltages under variable reference current conditions. As illustrated, a perfect balancing of the DC link capacitors voltage has been

occurred with minimum voltage fluctuations as depicted in Figure II.30, where the load current tracks its reference and kept a perfect sinusoidal form with less harmonics as presented in Figure II.31.

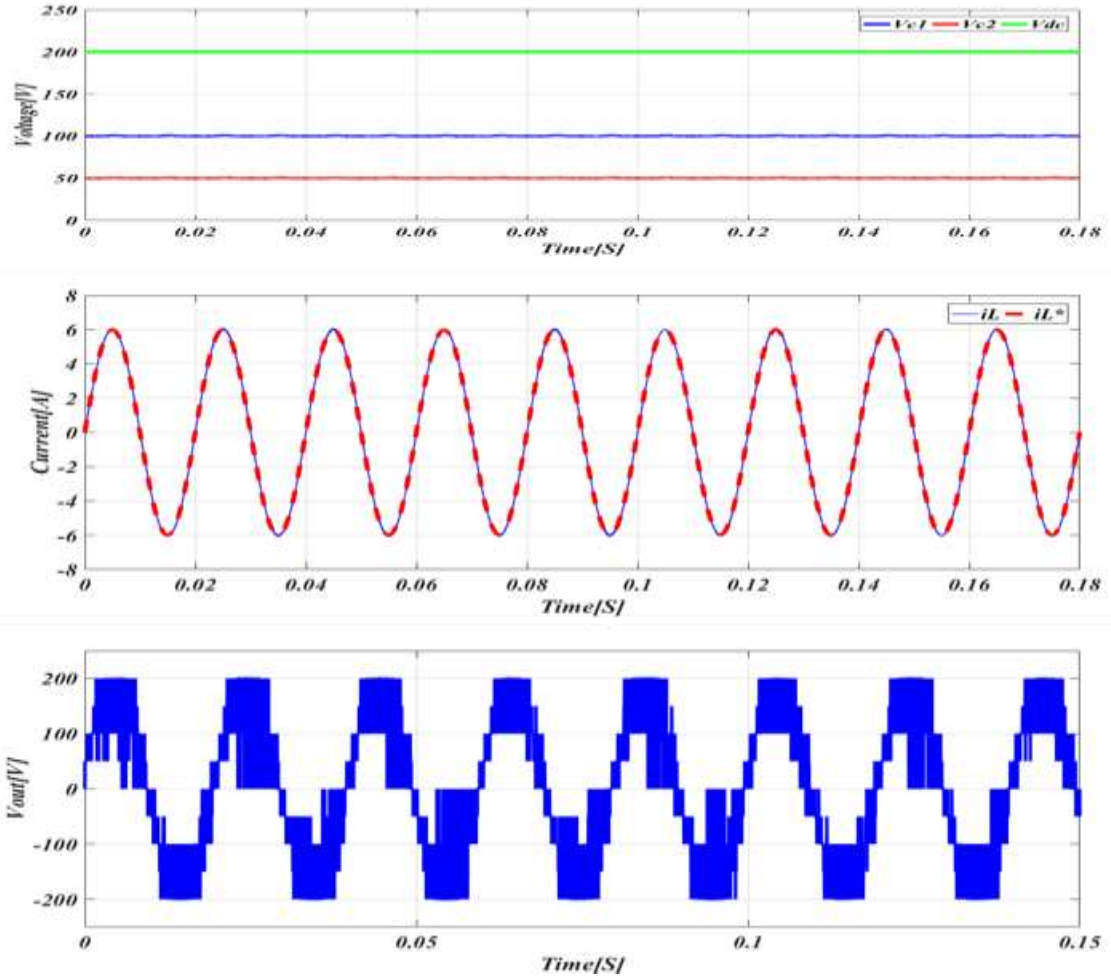


Figure II.28: Simulation results of PUC9 operation under fixed load condition using MPC

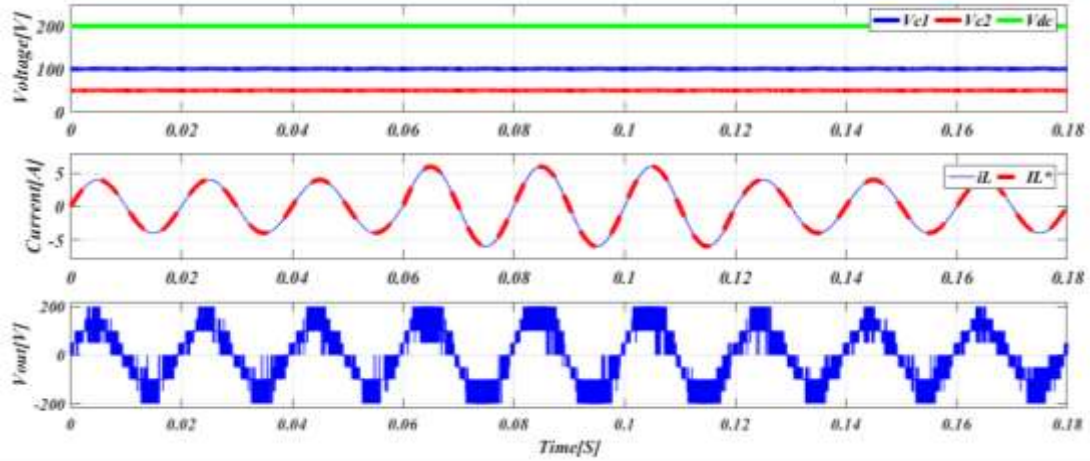


Figure II.29: Waveforms of capacitors voltage, load current and five-level output voltage under current variation using MPC

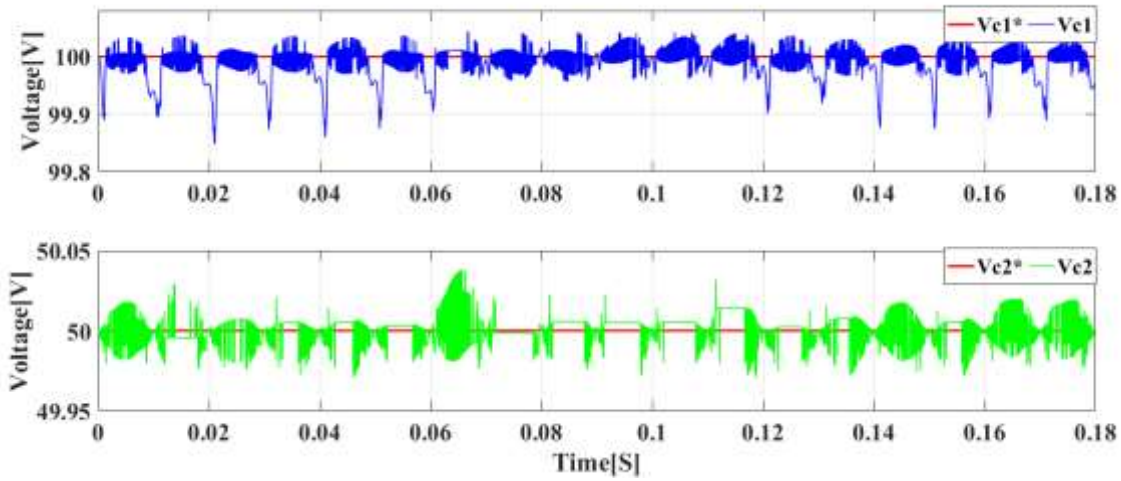


Figure II.30: Zoom of the DC link capacitors voltage using MPC

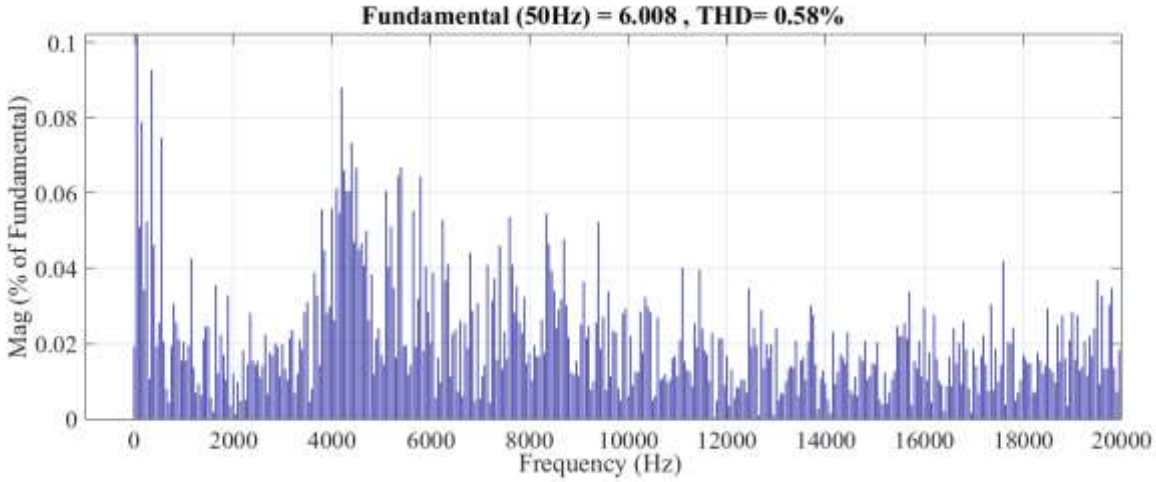


Figure II.31: THD analysis of load current

Table II.6 illustrates a comparison between the obtained results of proposed system using MPC and the conventional control technique, where the MPC shows their superiority in terms of DC link capacitor voltages balancing and harmonic elimination.

Table II.6: Comparison between PI with PWM and MPC

	THDi (%)	DC link capacitors voltage fluctuations (V)	
		C1	C2
Regulator PI with PWM	4.19	1.55	0.92
Controller MPC	1.43	0.195	0.07

b) Test 2: Grid-Connected Mode

In this test, the PUC9 inverter is connected to a single-phase AC source where the output voltage of the inverter must be greater than the grid voltage to achieve active power injection to the grid. The output voltage of the inverter V_{out} has a peak value of 200V, while the grid voltage has a peak value of 150V.

Figure II.32 (a) & (b) shows the response of the proposed system using the conventional control technique-based on a PI controller and a PWM modulator. The DC link capacitors voltage shows a perfect balancing with a very small fluctuation around their reference as illustrated in Figure II.33, the grid current in steady and variable conditions of grid current reference, has a sinusoidal from and well synchronized with the grid voltage with low THD as presented in Figure II.34, the nine-level voltage waveform has been obtained easily at the inverter output and has a symmetrical shape.

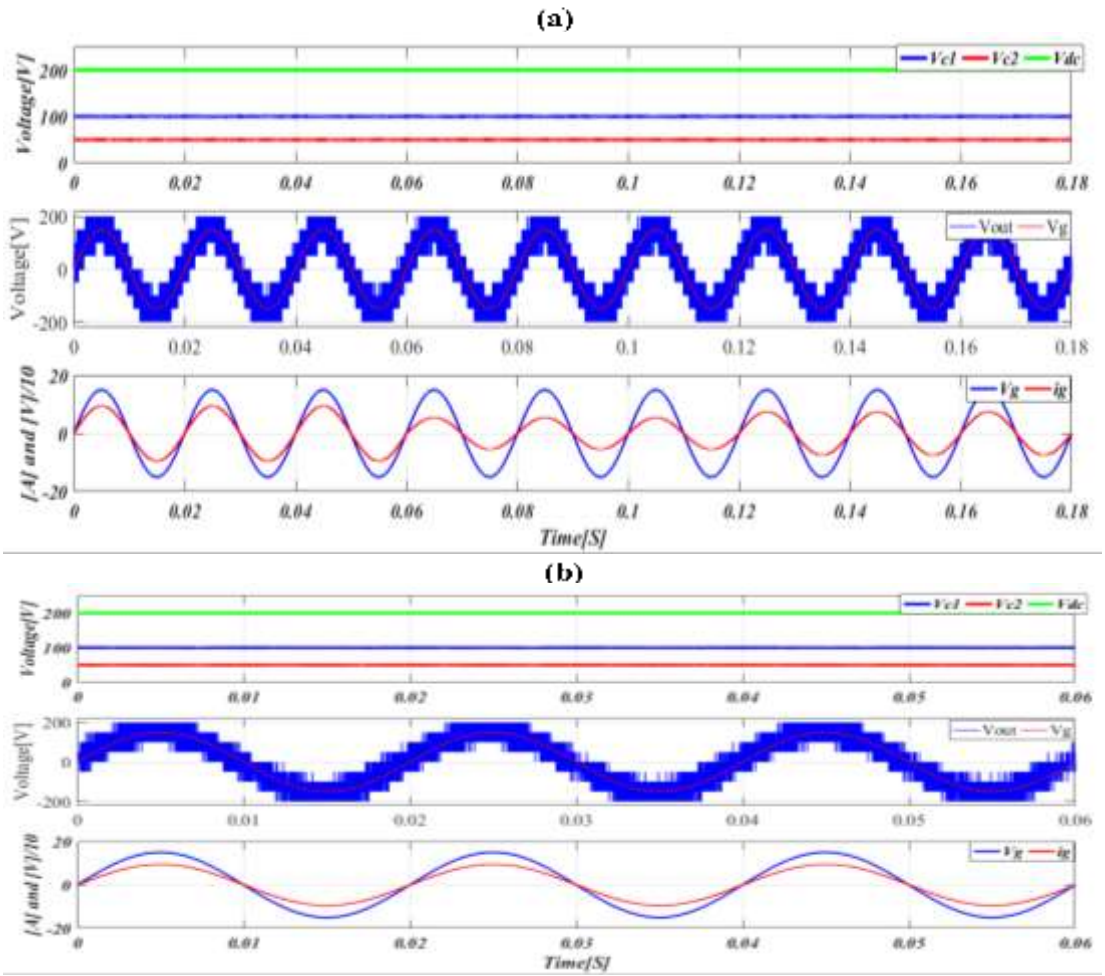


Figure II.32: Waveforms of DC link capacitor voltage, nine level output voltage and grid current and voltage: (a) under grid current reference variation, (b) under fixed grid current reference using PI with PWM

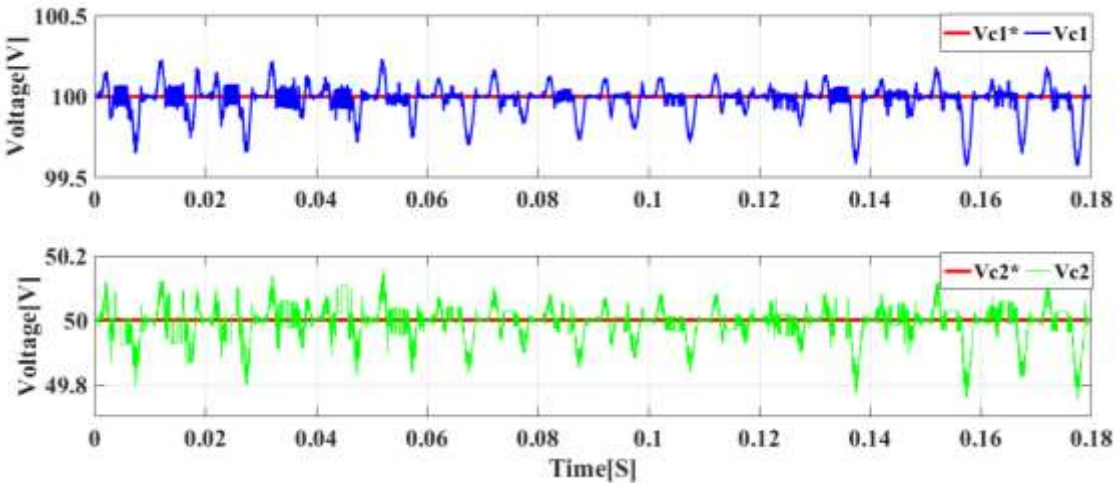


Figure II.33: Zoom of the DC link capacitors voltage using PI with PWM

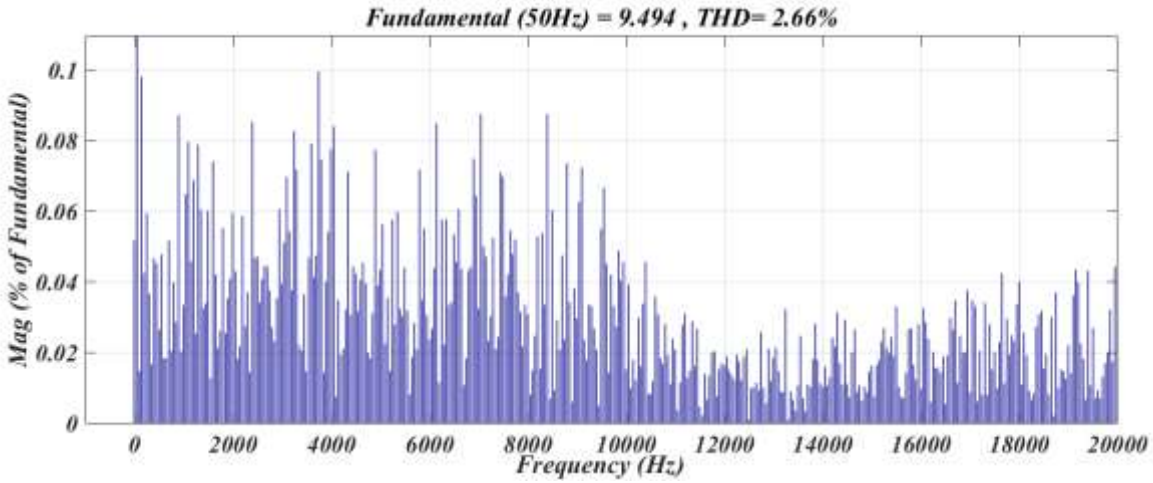


Figure II.34: THD analysis of the grid current.

Figure II.35 (a) & (b) illustrates the obtained results of the proposed topology response using MPC control strategy. From the obtained results we can observe that the DC link capacitors are well balanced with a very small fluctuation as presented in Figure II.36, the good balancing of the DC link capacitors voltage allows to obtain a very good and symmetrical nine level output voltage regardless of the current reference variations, on the other hand the grid current ig shows a sinusoidal form with very less harmonic values (Figure II.37) and with a perfect synchronization with the grid voltage, which prove the high dynamic performance of the proposed MPC strategy.

Table II.7 Illustrates a comparison between the obtained results between the proposed system using MPC and the conventional control technique in terms of current quality and DC link capacitors voltage fluctuations. From the obtained results we can observe the superiority

of the proposed MPC compared to the conventional control strategy in terms of harmonics elimination and DC link capacitors voltage balancing.

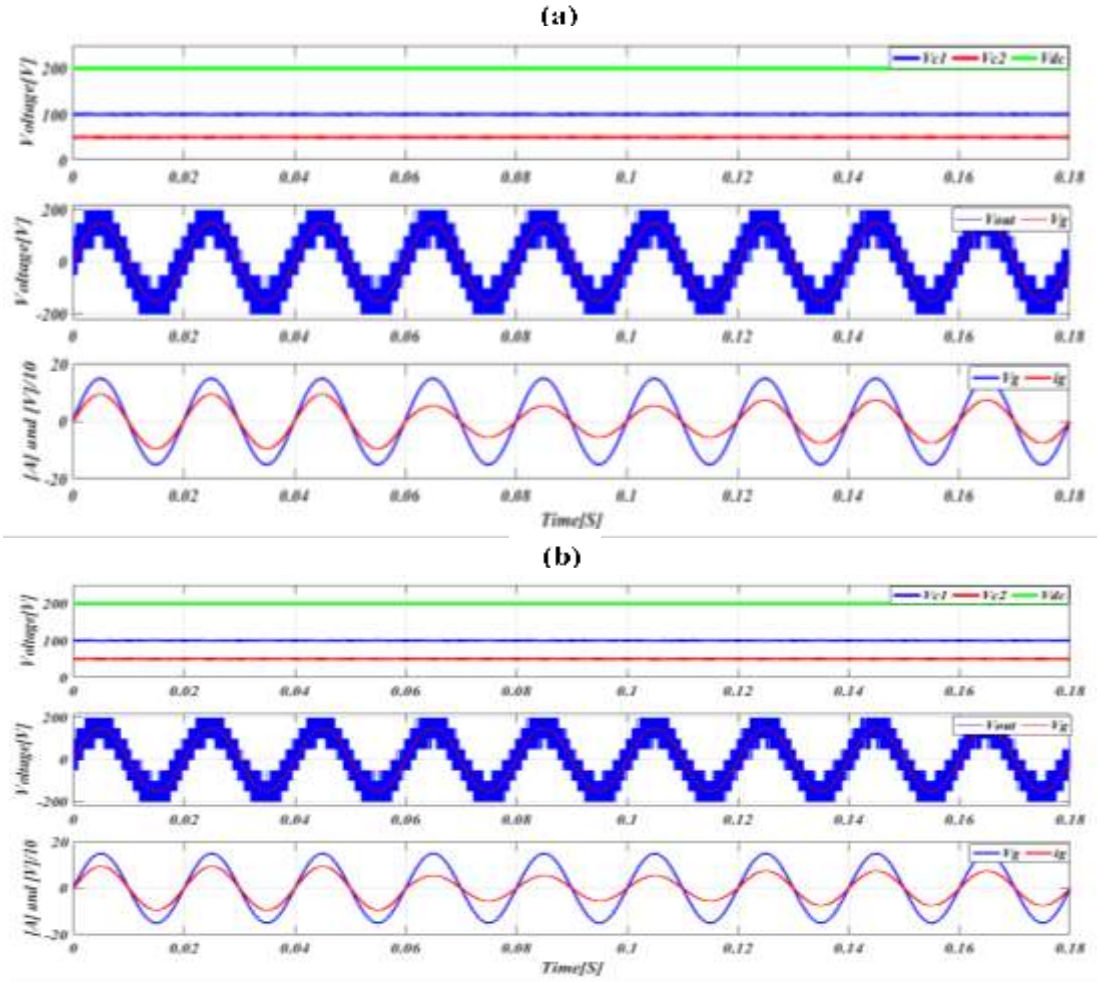


Figure II.35: Waveforms of DC link capacitor voltage, nine level output voltage and grid current and voltage: (a) under grid current reference variation, (b) under fixed grid current reference using MPC

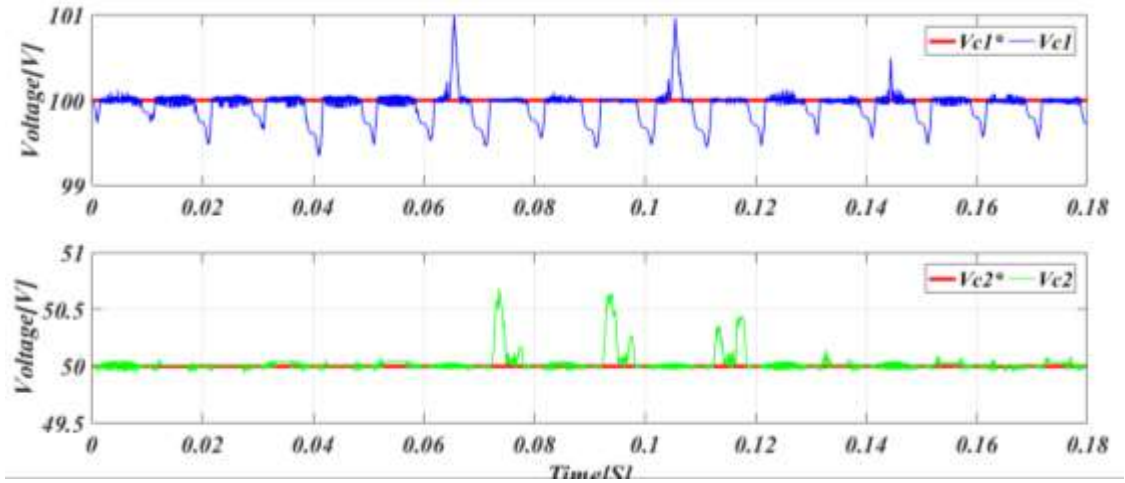


Figure II.36: Zoom of the DC link capacitors voltage using MPC.

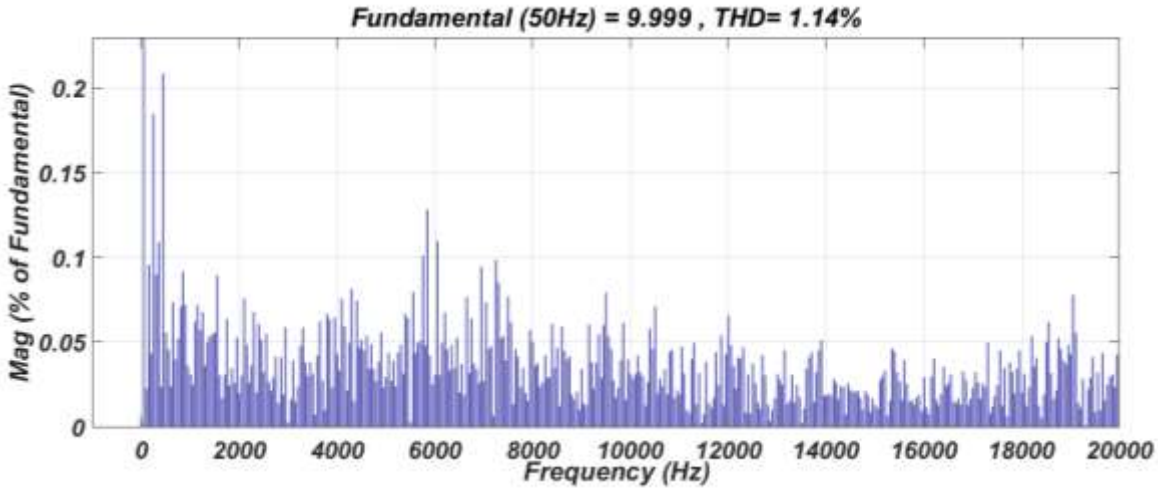


Figure II.37: THD analysis of the grid current.

Table II.7: Comparison between PI with PWM and MPC.

	THDi (%)	DC link capacitors voltage fluctuations (V)	
		C1	C2
Regulator PI with PWM	2.66	0.66	0.4
Controller MPC	1.14	1.64	0.74

II.6. Comparison between PUC inverter and two-level inverter

Table II.8 and II.9 illustrate a summary of the current THDi analysis and the voltage THDv of the inverter output obtained from using MPC and conventional PI with PWM control strategies with different inverter topologies used in this chapter in grid connected application. All the obtained results have been compared with the conventional two-level inverter in order to demonstrate the superiority of the proposed multilevel inverters topologies.

Table II.8: Comparison between simple two-level and PUC five nine-level signal phase inverter with MPC

Control strategy	Model predictive control **(MPC)**		
Signal phase inverter	Simple Two-level	PUC five-level	PUC nine-level
THDi (%)	2.76	1.43	1.14
THDv (%)	82.46	40.38	32.71

Table II.9: Comparison between simple two-level and PUC five nine-level signal phase inverter with PI and PWM

Control strategy	PI with PWM		
Signal phase inverter	Simple Two-level	PUC five-level	PUC nine-level
THDi (%)	4.97	4.19	2.66
THDv (%)	157.71	130.30	81.69

From these tables, we can conclude that the PUC9 inverter demonstrate a very high quality in terms of current and voltage harmonics. On the other hand, the proposed MPC shows better results compared to the conventional PI with PWM control.

II.7. Conclusion

In this chapter, analytical studies have been carried out for multilevel inverters topologies PUC5 and PUC9 inverters with different control strategies; a conventional PI with PWM and MPC control strategies. The main goal is to bring out the benefits of multilevel inverters in terms of current losses limitation and voltage fluctuations, where different DC link capacitors voltage balancing techniques have been studied and tested for both inverter topologies. The obtained results shows that model predictive control strategy is the most suitable current control technique for multilevel inverters; on the other hand nine level PUC9 inverter demonstrate a very high capabilities in terms of current harmonics elimination and voltage fluctuations compared to five level PUC5 inverter or two-level inverter.

Conclusions

In this thesis, analytical studies have been carried out for multilevel inverters topologies PUC5 and PUC9 with different control strategies; a conventional PI with PWM and MPC control strategies. The PUC5 topology with three pairs of switches can generate five different voltage levels, and PUC9 with four pairs of switches can generated nine voltage levels. On the other hand, MPC is a simple and intuitive method that does not have confusing gains to adjust as well as featuring fast response during any change in the system parameters.

The simulation results demonstrate that the implemented MPC controllers have fast response on signal phase multilevel PUC inverters with high current quality compared with the strategy based on PI with PWM. In addition, the DC link capacitor voltages are seen to be regulated at the desired levels, and five and nine-level voltage waveforms have been formed at the inverters outputs.

The following future research works are suggested as an extension to the knowledge presented in this thesis:

- Comparison of MPC controllers with other control techniques.
- Performance improvement of the predictive strategy, where more investigations are needed such as weighting factor selection and variable switching frequency.

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ABSTRACT

This thesis describes a grid-connected system with five and nine level PUC topologies using a Model Predictive Control (MPC) technique. The studied system consists of a single phase multilevel inverter with three pairs of switches for PUC5 and four pairs for PUC9 that work in a complementary matter. These topologies have the ability to generate five and nine different voltage levels with less number of active and passive components comparing with conventional multilevel inverter topologies. The suggested control technique (MPC) aims at reducing the total harmonic distortion (THD) of the grid injected current compare with conventional control while balancing the capacitors' voltages at their nominal reference values. Robustness analysis of the proposed model including the effect of a step change in the injected current into the grid. Theoretical analysis, mathematical modelling and simulation results using Matlab/Simulink software are presented in this thesis. The PUC5 THD of the injected current for the MPC is 1.43%, and 1.14% with PUC9.

Résumé

Cette thèse décrit deux topologies PUC à cinq et à neuf niveaux connectées au réseau à l'aide d'une technique de modèle de contrôle prédictif (MPC). Le système étudié se compose d'un onduleur monophasé à plusieurs niveaux avec trois paires d'interrupteurs à PUC5 et quatre paires à PUC9 qui fonctionnent de manière complémentaire. Ces topologies ont la capacité de générer cinq et neuf niveaux de tension différents avec moins de composants actifs et passifs par rapport aux topologies d'onduleurs multiniveaux classiques. La technique de contrôle suggérée (MPC) vise à réduire la distorsion harmonique totale (THD) du courant injecté dans le réseau par rapport au contrôle conventionnel tout en équilibrant les tensions des condensateurs à leurs valeurs nominales de référence. Analyse de robustesse du modèle proposé incluant l'effet d'un changement progressif du courant injecté dans le réseau. Les résultats de l'analyse théorique, de la modélisation mathématique et de la simulation à l'aide du logiciel Matlab/Simulink sont présentés dans cette thèse. Le THD du courant injecté pour le modèle proposé avec PUC5 est de 1,43%, et 1,14% avec PUC9.

ملخص

تصف هذه الأطروحة طوبولوجيا PUC ذات خمسة وتسعة مستويات متصلة بشبكة باستخدام تقنية التحكم التنبئي النموذجي (MPC) .يتكون النظام المقترح من عاكس متعدد المستويات أحادي الطور مع ثلاثة أزواج من المفاتيح في PUC5وأربعة أزواج في PUC9 ، ومصدر واحد للتيار المستمر ومكثف مع خمس مستويات ومكثفتين في تسعة متصلة بالشبكة. تتمتع هذه الهيكلية بالقدرة على توليد خمسة وتسعة مستويات مختلفة من الجهد مع عدد أقل من المكونات مقارنة بطوبولوجيا العاكس التقليدية متعددة المستويات. تهدف تقنية التحكم المقترحة (MPC) إلى تقليل التشوه التوافقي الكلي (THD)للتيار المضخ بالشبكة مقارنة مع التحكو التقليدي PID مع موازنة جهود المكثفات في قيمها المرجعية. تم إجراء تحليل المتانة للنموذج المقترح بما في ذلك تأثير تغيير الخطوة في التيار المضخ في الشبكة .يتم تقديم التحليل النظري والنمذجة الرياضية ونتائج المحاكاة باستخدام برنامج Matlab / Simulink في هذه الأطروحة. إنPUC5 THD للتيار المضخ للنموذج المقترح هو 1.43٪ ، و 1.14٪ معPUC9 .